Report of

STTP

Organized By Electronics & Communication Engineering Department

Parul Institute of Engineering & Technology (Diploma Studies)

On

"Recent Trends in Embedded Systems, VLSI Designing & Power Electronics"

16-18 October, 2011

Parul Institute if Engineering & Technology(Diploma Studies)

Accrediated by NBA, AICTE

(In association with Parul Institute of Engineering & Technology, Parul Institute of Technology & Parul Polytechnic Institute)

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In the era of fast growing technology, short term training program (STTP) plays a significant role in synchronizing and keeping up with the current global trends. The objective of this course was to create awareness among faculty members, research scholars, students, industry and R & D personnel to understand the importance and requirements in emerging field of Embedded system, VLSI Designing and Power Electronics. The course was designed to introduce participants to the trends in this emerging field.

Major Thrust Areas Targeted

- ARM Processor Instruction Set & Programming
- Penetration of Android in Embedded Domain
- Recent Trends in Power Electroincs
- Application Specific Integrated Circuit - ASIC Design
- Application of Evolutionary Algorithm in VLSI
    (1) Automatic Circuit Design
    (2) MOSFET Parameter Extraction
- Embedded System design, Trends and Challenges
- Power Basic, Logic Power, Low Power Design

The STTP was inaugurated by **Dr. C.H.Vithalani,** Head, EC Engineering Department, Government Engineeing College, Rajkot, at 10:45 AM on 16th October, 2011 in the Auditorium Hall of Parul Institute. The Inaugural function was presided by Dr. Jayeshbhai K. Patel, Chairman, Parul Arogya Seva mandal and Prof. (Mrs.) Archana S. Nanoty, Principal of Parul Institute of Engineering and Technology (Diploma Studies) and **Mr. Prajose John,** Traing - Manager, e-Infochip, Ahmedabad. The theme of STTP was explained by Prof. (Mrs.) Archana S. Nanoty. Dr. C.H.Vithalani discussed in detail the importance of Embedded Systems, VLSI designing and Power Electronics. Mr. Umang Soni, Convener,Head, EC Department, Parul Institute of Engineering and Technology (Diploma Studies) extended Vote of thanks to the dignitaries and staff members who helped to organize the STTP.

There were 78 entries from all over the Gujarat to attend the STTP. As per their feedback at the end of STTP, the purpose of organizing this STTP was fulfilled to their utmost satisfaction. **Dr. Dipankar Nagchoudhuri**, Distinguished Professor, Dhirubhai Ambani Institute of Information & Communication Technology, Ahmedebad and Mr. Prajose John, Training-Manager, e-Infochip, Ahmedebad were some of the prominent personalities among the resource persons who contribute to the success of the STTP. Certificate and CD of course materials are given to each participant.

SCHEDULE

Short Term Training Programme

On

Recent Trends in Embedded Systems, VLSI Designing & Power Electronics"

16-18 October, 2011

Parul Institute of Engineering & Technology (Diploma Studies)

Schedule of Lecture (E.C. Engg. Dept.)

DAY	NAME OF RESOURCE PERSON	DESIGNATION & ORGANIZATION	DATE	TIME	TOPIC
1	Dr. C. H. Vithalani	Head, EC Dept., Government Engineering College, Rajkot	16.10.2011	11:00AM to 1:00PM	"ARM Processor Instruction SET & Programming"
	Mr. Prajose John	Training Manager from e-Infochips Ltd.	16.10.2011	2:00PM to 3:15PM & 3:30PM to 4:30PM	"Penetration of Android in the Embedded Domain"
2	Mr. M. R. Tilwali	Proprietor, Gururaj Engineering, Vadodara	17.10.2011	10:30AM to 12:30PM	"Recent Trends In Power Electronics"
	Dr. D. Nagchoudhuri	Distinguished Professor, DAIICT, Gandhinagar	17.10.2011	1:30PM to 3:30PM	"ASIC Design"
	Prof. Rajesh A. Thakker	Associate Professor – EC, Vishwakarma Govt. Engg. College, Chandkheda, Gandhinagar	17.10.2011	3:45PM to 5:45PM	"Applications of Evolutionary Algorithms in VLSI: Automatic Circuit Design and MOSFET Parameter Extraction"
3	Mr. Madhukant Patel	Chairman, IETE Ahmedabad, CTO, IMP Consultancy, Former Scientist/ Engineer ISRO	18.10.2011	10:30AM to 12:30PM	"Embedded System Designs, Trends & Challenges"
	Prof. A. D. Darji	Assistant Professor from S.V.N.I.T., Surat	18.10.2011	1:30PM to 3:30PM	"Power Basic, Logic Power, Low Power Design"

DAY-1

Dr. Jayeshbhai K. Patel, Chairman, Parul Arogya Seva Mandal, Prof. Archana S. Nanoty, Principal of P.I.E.T.(D.S.), Dr. C. H. Vithalani, Head, EC Department, G.E.C., Rajkot, Mr. Prajosh John, Training Manager, E-Infochip, Ahmedabad lightening lamp

Dignitaries on the dias during the Inauguration function of STTP on **"Recent Trends in Embedded system, VLSI Design and Power Electronics"**

Dr. Jayeshbhai K. Patel, chairman, Parul Arogya Seva Mandal, giving the speech.

Prof. Archana S. Nanoty, Principal of Parul Institute of Engineering & Technology (Diploma Studies), giving the welcome speech

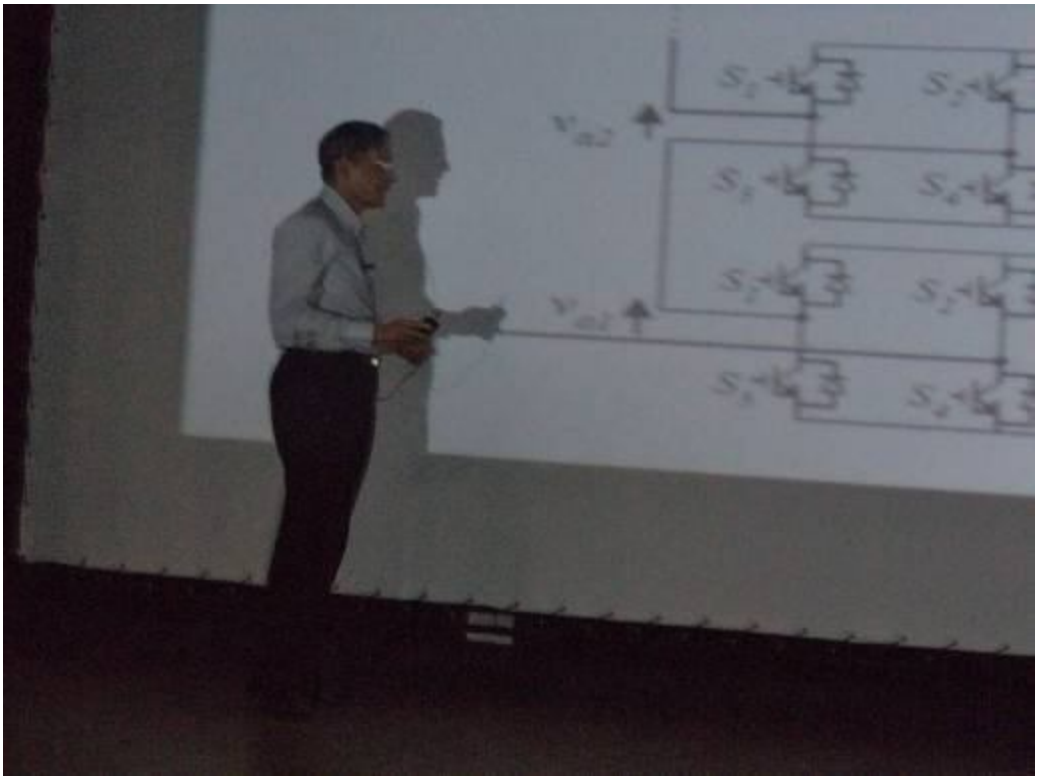
Dr. Jayeshbhai K. Patel, chairman, Parul Arogya Seva Mandal presenting memento to Dr. C.H. Vithalani.

Dr. Jayeshbhai K. Patel, chairman, Parul Arogya Seva Mandal presenting memento to Mr. Prajosh John

Key Note Speaker, Dr. C.H. Vithalani, Head, EC Dept., Government Engineering College, Rajkot delivering lecture on **"ARM Processor Instruction Set & Programming"**

Mr. Prajose John training manager from e-Infochips Ltd. Delivering lecture on **"Penetration of Android in the Embedded Domain"**

DAY-2



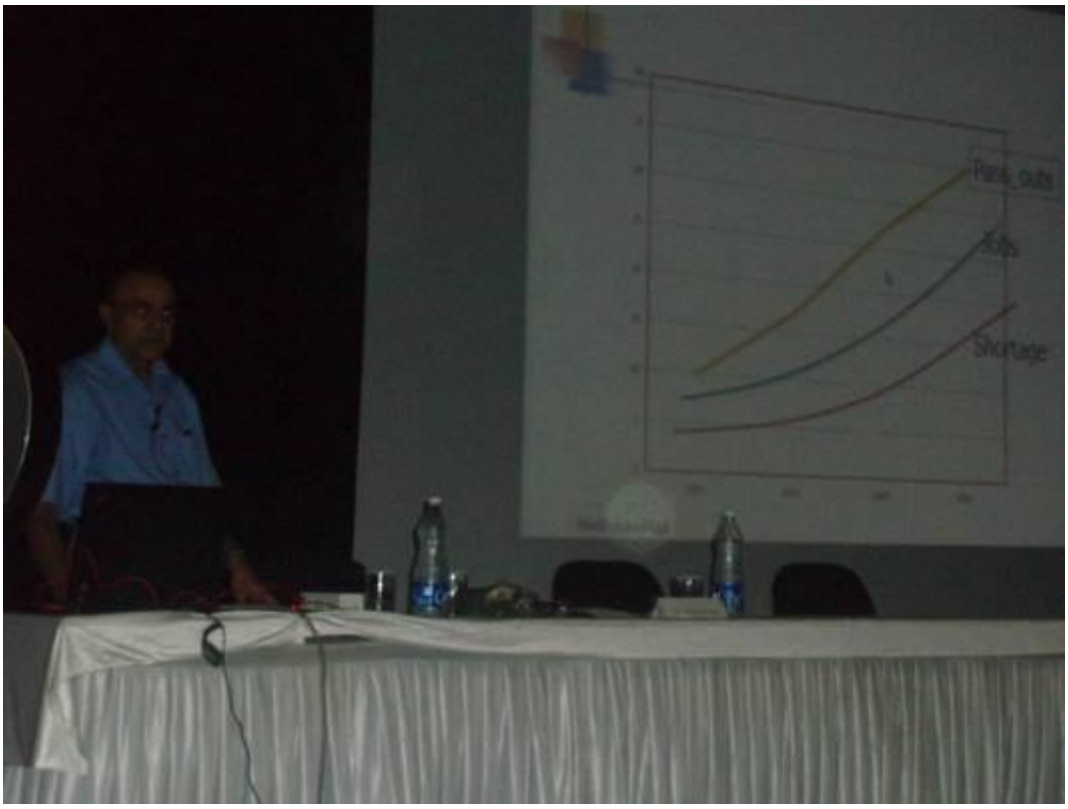
Mr. M.R.Tilwali, Proprietor, M/S Gururaj Engineers, Vadodara delivering lecture on **"RECENT TRENDS IN POWER ELECTRONICS"**

Dr. D. Nagchoudhuri, Distinguished Professor, DAIICT, Gandhinagar delivering lecture on **"ASIC DESIGN"**

Prof. Rajesh A. Thakker, Associate Professor – EC Dept., Vishwakarma Govt. Engg. College, Chandkheda, Gandhinagar delivering lecture on **"Applications of Evolutionary Algorithms in VLSI: Automatic Circuit Design and MOSFET Parameter Extraction"**

Participants attending the Session

DAY-3



Mr. Madhukant Patel, Chairman, IETE Ahmedabad, CTO, IMP Consultancy, Former Scientist/ Engineer ISRO delivering lecture on **"Embedded System Designs, Trends & Challenges"**

Prof. A.D.Darji, Assistant Professor from S.V.N.I.T., Surat delivering lecture on **"Power Basic, Logic Power, Low Power Design"**