Certificate from Sponsoring Authority

Certified that the above applicant is employed in our organization and the information stated by him/her has been verified and found correct. We sponsor him/her for attending Workshop.

Date:
Place:

Signature of sponsoring authority with seal

Please send the duly filled application form to:

Prof. N. D. Patel/Prof. P. P. Gandhi
Electronics &
Communication Engineering Department
L.C. Institute of Technology
Mehsana- Unjha Highway
At & Po: Bhandu- 384120
Dist: Mehsana
Gujarat - India

Tel: (02765) 287145 (0)- 151
Mob: +919879381145,+919825440134
Fax: (02765) 287945
Email: ec.hod@lcit.org

Important Dates:
Receipt of Application : 17/01/2011
Confirmation of Selection
by Email/Website : 20/01/2011
Commencement of course: 28/01/2011

Eligibility for Admission

Faculty form EC, CE, CSE, IC Engineering background & professionals from various Research Organizations & industries working in same area.

Advisory Committee

Dr. D. J. Shah, Principal LCIT, Bhandu
Prof. J. V. Dave, Principal GEC, Gandhinagar.
Dr. N. M. Devashrayee, PG Coordinator, VLSI Design, Nirma University, Ahmedabad
Prof. S. S. Patel, Dean EC & EE, LCIT, Bhandu
Mr. Brijesh Shah, Ni2 Design, Pune

Resource Person

Course will be conducted by senior & experienced faculty from the various renowned institutes like DA-IICT- Ghandhinagar, Nirma University- Ahmedabad & Eminent Experts form Research Organization and Industries working in this area.

Course Fee & Registration

- Rs.250/- for ISTE Faculty Members & PG, Ph.D Students
- Rs.500/- for Non- ISTE Members
- Rs.1000/- for Candidates form Industry
- Accommodation on paid basis will be provided.

How to apply

Interested faculty members form Engineering colleges, polytechniques and industry are requested to fill up the attached application form and return it to the Coordinator, so as to reach on or before January 17, 2011. Applicant should send the Demand Draft in favour of "Principal L.C. Institute of Technology", payable at Mehsana

ISTE
INDIAN SOCIETY FOR TECHNICAL EDUCATION

ISTE Approved
National Workshop
On

Mixed Signal VLSI Design

28-29 January, 2011

Co-ordinator
Prof. Nilesh D. Patel

Co-Coordinator
Prof. Priyesh P. Gandhi

LCIT
ESTD - 2002

:: Organized by ::

Department of Electronics & Communication Engineering
Laljibhai Chaturbhai Institute of Technology
Mehsana –Unjha Highway, Bhandu-384120
Dist: Mehsana (Gujarat)
Website: www.lcit.org
Tel (O): 02765-287145,287368 Fax: 02765-287945

LCIT

Laljibhai Chaturbhai Institute of Technology nurtures the intellectual growth of its students and serve humanity through creation, application, and dissemination of knowledge relevant to technology and become one of the premier engineering college and achieve the highest order of excellence in teaching & learning.

The Laljibhai Chaturbhai Institute of Technology, Bhandu (LCIT) represents a shared vision and a collaborative effort of Mr. Bhogilal Laljibhai Patel and his team of committed professionals and family members. This vision began to take form as early as 1978 when our present Chairman Mr .Bhogilal Patel decided to open social service centers and educational institutions in his native place Valam, a tiny village, nestled in the milk district of Mehsana in Gujarat State of India. Several years later in 2002 the LCIT was established close to this village to actively pursue and make this vision a reality.

The campus is situated on a beautifully landscaped 25-acres land at Bhandu.

About Department

Department of Electronics & Communication is enriched with latest equipments like DSP Kits and Emulator, Spectrum Analyzer, DSO, PIC Microcontroller Kits and Software's like MATLAB, Multisim, Quatrus- II, Embedded Systems, Fiber Optics, CCS. etc. The department has state of art laboratories and necessary facilities to enhance the quality of teaching- learning process.

Organizing Secretary

Prof. M. L. Patel
Prof. H. D. Nayak

Organizing Committee

Prof. H. L. Judal
Prof. A. D. Dobariya
Prof. S. K. Patel

Objective of the Program

The course is intended to acquaint the participants from the basics of Mixed Signal VLSI Design to the advance trends. The course is aimed to familiarize the participants about the various advanced methods used for Low Power, High Speed VLSI Designs, Testing and Verification of the design as per the industry perspective. Hands- on sessions are also designed to supplement the class room discussions. The simulation of various Back End VLSI Designs, writing of Test Benches will be demonstrated with hands on in Laboratory sessions.

Course Content

- Low Power VLSI Design
- High Speed VLSI Design
- Testing & Verification
- Digital VLSI Design
- Analog VLSI Design
- FPGA Based Design
- Back End VLSI Design
- PSoC
- Laboratory Sessions

Registration Form

ISTE Approved
National Workshop
On
Mixed Signal VLSI Design
28– 29 January, 2011

Name (Prof./Mr./ Ms.) : _____

Designation : _____

Qualification : _____

Experience (1) Teaching : _____

(2) Industry : _____

Name of the Institute/ Industry :_____

Mailing Address(with Phone & Fax No) :

_____

_____

_____

E- mail :_____

ISTE Membership No: _____

Accommodation Required / Not Required

DD Details: Amount: _____ No:_____
Name of the Bank: _____ Dated: _____

Date: _____
Place: _____

Signature of Applicant