GUJARAT TECHNOLOGICAL UNIVERSITY

B E Sem-VI Examination May 2011

Subject code: 161004   Subject Name: VLSI Technology and Design
Date:21/05/2011   **Time: 10.30 am – 01.00 pm**
                                                             Total Marks: 70

Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Discuss fabrication process of NMOS transistor.   **07**
        (b) Why is the size of PMOS transistor chosen to be 2.5 times of an NMOS transistor?   **03**
        (c) Discuss VLSI design flow in detail   **04**

Q.2 **(a)** Explain the band diagram of MOS Structure at surface inversion and derive the   **07**
               expression for threshold voltage.
        (b) Consider a MOS system with the following parameters: **07**
               $t_{ox} = 200A°$,
               $\Phi_{GC} = - 0.85$ V,
               $N_A = 2*10^{15}$ cm^{-3},
               $Q_{ox} = q * 2 *10^{11}$ C/cm^2
               1) Determine the threshold voltage V under zero bias at room temperature
                   (T = 300 °K). Note that ε_{ox}=3.97ev and ε_{si}=11.7ev.
               2) Determine the type (p-type or n-type) and amount of implant.

OR

        (b) Design of a depletion-load NMOS inverter: **07**
               $\mu_n c_{ox} = 30$ μA/V^2 ,
               $V_{T0} = 0.8$ V (enhancement-type),
               $V_{T0} = - 2.8$ V,(depletion-type),
               $\gamma = 0.38$ V$^{1/2}$,
               $|2 \Phi_F| = 0.6$ V,
               $V_{DD} = 5$ V.
               1) Determine the (W/L) ratios of both transistors such that:
                   i)   the static (DC) power dissipation for $V_{in} = V_{OH}$ is 250 μW, and
                   ii) $V_{OL} = 0.3$ V.
               2) Calculate V_{IL} and V_{IH} values, and determine the noise margins

Q.3 **(a)** With neat sketch explain gradual channel approximation and derive the equation   **07**
               for drain current in linear region mode and saturation mode.
        (b) Effect of channel length modulation and substrate bias on drain current of NMOS   **07**
               transistor.

OR

Q.3 **(a)** Explain the basic principles of pass transistor circuits. Also explain logic "o" and   **07**
               logic "1" transfer.

        (b) By taking suitable examples, discuss the ratioed and ratio-less dynamic logic   **07**
               circuits.

Q.4 **(a)** Draw circuit of resistive load inverter. Derive V_{IH}, V_{IL}, V_{OL} and V_{OH} for resistive load inverter.   **07**

(b) Consider a CMOS inverter circuit with the following parameters: **07**
$V_{DD} = 3.3$ V,
For NMOS $V_{TO, n} =$ 0.6 V, $\mu_n C_{ox} = 60 \, \mu \, A/V^2$,   (W/L)n=8
For PMOS $V_{TO, p} = -0.7$ V, $\mu_p C_{ox} = 25 \, \mu \, A/V^2$,   (W/L)p=12.
Calculate noise margin and V_{th} of the circuit.

OR

Q.4 **(a)** Explain the principles of dynamic logic circuits.   **07**
(b) Derive threshold voltage equation for short channel effect.   **07**

Q.5 **(a)** How will you calculate propagation delay times tp_{HL} and tp_{LH} for CMOS Inverter?   **07**
(b) Ad hoc Testable design techniques   **07**

OR

Q.5 **(a)** Explain CMOS transmission gate.   **07**
(b) Explain Latch up problem in CMOS inverter. Mention causes and remedy for avoiding latch up.   **07**

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