Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (OLD) - EXAMINATION – SUMMER 2017

Subject Code: 161004 **Date: 10/05/2017**

Subject Name: VLSI Technology and Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain VLSI design flow with necessary diagrams.	**07**
	(b)	Realize below logic function using cmos logic gate. Also draw stick-diagram layout. Z = (A(D+E)+BC)'.	**07**
Q.2	**(a)**	Explain fabrication of the nMOS transistor with necessary diagrams.	**07**
	(b)	Describe the analysis of two-input nor gate using depletion nMOS loads.	**07**
		OR	
	(b)	Describe the analysis of CMOS inverter.	**07**
Q.3	**(a)**	Explain metal oxide semiconductor (MOS) structure.	**07**
	(b)	Describe the analysis of resistive load inverter.	**07**
		OR	
Q.3	**(a)**	Write shot note on MOSFET scaling and small-geometry effects.	**07**
	(b)	Describe the analysis of inverter with n-type MOSFET load.	**07**
Q.4	**(a)**	Explain calculation of interconnect delay.	**07**
	(b)	Explain voltage bootstrapping in dynamic circuit.	**07**
		OR	
Q.4	**(a)**	Explain interconnect capacitance estimation.	**07**
	(b)	Explain CMOS transmission gate logic.	**07**
Q.5	**(a)**	Write short note on CMOS D-latch.	**07**
	(b)	Write short note on latch-up and its prevention.	**07**
		OR	
Q.5	**(a)**	Write short note on Ad-Hoc testable design techniques.	**07**
	(b)	Write short note on FPGA and CPLD.	**07**

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