Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII (OLD) - EXAMINATION – SUMMER 2017

Subject Code:180802 **Date:29/04/2017**

Subject Name: VLSI Technologies

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss VLSI design flow in brief.	**07**
	(b)	Explain fabrication process of nMOS transistor with diagram.	**07**
Q.2	**(a)**	Draw and explain Energy band diagram of a p-type silicon substrate.	**07**
	(b)	Discuss basic steps of the LOCOS Process.	**07**

OR

Q-2	**(a)**	What is enhancement-mode MOSFET and depletion-mode MOSFET? Explain in detail.	**07**
	(b)	Draw and explain the structure of MOS.	**07**
Q.3	**(a)**	Explain any one down scaling techniques for MOSFET.	**07**
	(b)	Derive the equation of Threshold voltage of MOS Structure.	**07**

OR

Q.3	**(a)**	Explain Oxide-related Capacitances.	**07**
	(b)	Explain the depletion load nMOS inverter and derive equation of critical voltage points VOH, VOL, VIL and VIH	**07**
Q.4	**(a)**	Explain Noise immunity and noise margin using Inverter Example.	**07**
	(b)	Explain Voltage Bootstrapping.	**07**

OR

Q.4	**(a)**	Explain CMOS Transmission Gates (TGs) in detail.	**07**
	(b)	Explain basic principle of pass transistor with logic “1” transfer.	**07**
Q.5	**(a)**	Discuss Built-in Self Test (BIST) Techniques.	**07**

	(b)	Give comparison between FPGA and CPLD.	**07**
		OR	
Q.5	**(a)**	Explain Scan –based techniques in detail.	**07**
	(b)	Discuss Controllability and Observability.	**07**

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