Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2131004 **Date: 05/06/2017**

Subject Name: Digital Electronics

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **A** **Find correct answer from given choices.** **07**

1 The output of a ____ gate is only 1 when all of its inputs are 1
(a) NOR (b) XOR (c) AND (d) NOT

2 Which gate equivalent is to bubbled OR gate?
(a) AND (b) XOR (c) NOT (d) NAND

3 The digit F in Hexadecimal system is equivalent to —— in decimal system
(a)16 (b)15 (c)17 (d) 8

4 A NOT gate has…
(a) Two inputs and one output (b) One input and one output
(c) One input and two outputs (d) none of above

5 The digital logic family which has minimum power dissipation is
(a) TTL (b) RTL
(c) DTL (d) CMOS

6 $(734)_8 = (\ )_{16}$
(a) C1D (b) DC1
(c) 1CD (d) 1DC

7 1 Kb corresponds to _____
(a) 1024 bits (b) 1000 bytes (c)210 bytes (d) 210 bits

B **Define Following Terms** **05**

1. Positive Logic
2. Negative Logic
3. Fan In
4. Fan out
5. Noise Margin

C State and Prove D'Morgan Theorem. **02**

Q.2 **(a)** Convert the expression Y= A + BC into the standard SOP form. **03**

(b) Simplify Using boolean laws and draw the logic diagram for the simplified expression. **04**

$F = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C$

(c) Explain Full Subtractor with truth table and circuit diagram. **07**

OR

(c) Simplify following Boolean function by using the tabulation method **07**

$F = \Sigma(0,1,3,7,8,9,11,15)$

Q.3 **(a)** Explain magnitude comparator. **03**

(b) Prove that NAND gate as Universal gate. **04**

(c) Simplify following Boolean function using VEM. **07**

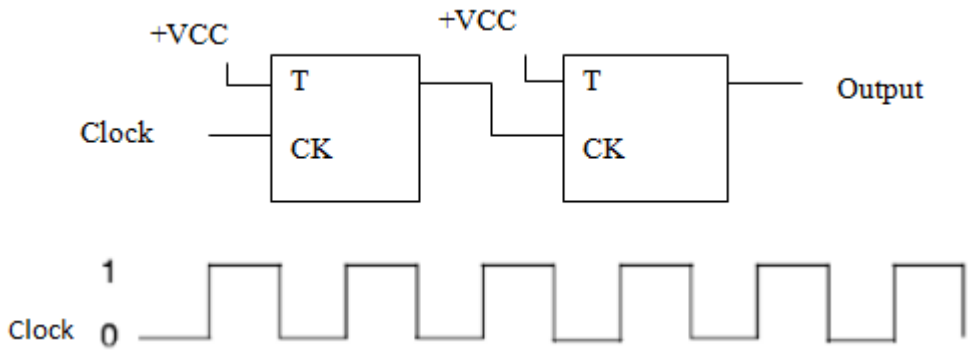
$F = AB'CD + A'BC'D + AB'CD' + A'B'C'D$

$F = A'B'C'D + A'BC'D' + A'BC'D + AB'C'D' + AB'CD' + AB'CD + ABCD'$

OR

Q.3 **(a)** State and Prove D'Morgan Theorem for three variables. **03**

	(b)	Convert the decimal number 250.5 to base 3, base 4, base 7 and base 8	**04**
	(c)	Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generates the 9's Complement of the input digit.	**07**
Q.4	**(a)**	What is multiplexer? With logic circuit and function table explain the working of 4 to 1 line multiplexer.	**03**
	(b)	Simplify Boolean function using K-Map $F(w,x,y,z) = \Sigma(1,3,5,8,9,11,15)$ $d(w,x,y,z) = \Sigma(2,13)$	**04**
	(c)	Implement following Boolean function using 8 : 1 multiplexer. $F(A,B,C,D) = \Sigma(2,3,5,7,8,9,12,13,14,15)$	**07**
		OR	
Q.4	**(a)**	State the advantages of Finite State Machine.	**03**
	(b)	Explain JK flip flop with its characteristic table and excitation table.	**04**
	(c)	Implement Full Subtractor Circuit with the help of Decoder and logic gates.	**07**
Q.5	**(a)**	Explain Master Slave JK flip-flop with truth table and circuit diagram.	**03**
	(b)	Draw and explain Ring counter	**04**
	(c)	Design a counter to generate the repetitive sequence 0, 1, 2,4,3,6.	**07**
		OR	
Q.5	**(a)**	Plot the out waveform referenced to the clock signal assuming the initial contents of the flip-flops is q=0. Assume all flip-flops are edge triggered.	**03**



	(b)	Write short note on Programmable Logic Arrays.	**04**
	(c)	Explain the Fundamental Mode Model of Asynchronous State Machine with suitable example	**07**

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