Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2131704 **Date: 05/06/2017**

Subject Name: Digital Logic Circuits

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			Marks
Q.1		Short Questions	14
	1	The 8-bit binary equivalent of decimal number 187 is A) $(010111011)_2$ B) $(11011101)_2$ C) $(10111101)_2$ D) $(10111100)_2$	
	2	Convert $(8B3F)_{16}$ to binary. A) 35647 B) 011010 C) 1011001111100011 D)1000101100111111	
	3	X=1010100 and Y=1000011. Using 2's complement, X-Y is, A) 10111 B)101101 C) 10011 D) 10001	
	4	What is noise margin in logic families?	
	5	Convert the following SOP expression to an equivalent POS expression ABC + AB'C' + AB'C + ABC' + A'B'C	
	6	Which gates are known as universal gates? Why?	
	7	What do you mean by negative edge triggered flip flop?	
	8	What is the difference between demultiplexer and decoder?	
	9	2 level AND- OR gate realization of a logic expression is equivalent to 2 level NAND- NAND gate realization. A) True B) False	
	10	D flip-flop stands for A)Dual flip flop B) Double flip flop C) Delay flip flop D) Derivative flip flop	
	11	What is the difference between Johnson counter and Ring counter?	
	12	List and state logic and shift microoperations.	
	13	Explain the term “Acquisition time “ with respect to ADC.	
	14	The fastest ADC is: A) Counter type A/D Converter B) Flash type A/D converter C) Dual slope A/D converter D) Successive approximation ADC.	
Q.2	(a)	Design full subtractor using K map and realize using logic gates.	03
	(b)	Minimize the following four variable logic function using K- map: f(A, B, C, D) = (A+B+C'+D') . (A'+C+D') . (A'+B+C'+D') . (B'+C) . (B' + C') (A + B') + (B' + D'). Realize the circuit using logic gates.	04
	(c)	Design BCD to Excess-3 code converter using k map. Draw circuit using logic gates.	07
		OR	
	(c)	Minimize the following function using tabulation method: F(w, x, y, z) = ∑ (1, 4, 6, 7, 8, 9, 10, 11, 15)	07
Q.3	(a)	Write a brief note on PLA(Programmable Logic Array).	03
	(b)	Explain the logic of look ahead carry generator in full adder with help of logic	04

diagram.

(c) Draw the logic diagram of 3:8 Decoder and write the truth table. Explain its operation. 07

OR

Q.3 (a) Explain the operation of master slave J-K flip flop. 03

(b) Design a counter that has a repeated sequence of six states as shown below in the table: 04

A	B	C
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

Draw the logic diagram and state diagram.

(c) Draw the logic diagram of clocked RS flip flop and explain its operation. 07

Q.4 (a) List out different types of memories used in digital logic circuits and define them. 03

(b) Explain the working of 4-bit Jhonson counter. Write the count sequence obtained at the output. 04

(c) Draw the logic diagram of 4-bit bidirectional shift register with parallel load and explain its operation. 07

OR

Q.4 (a) Explain floating point representation of numbers in register transfer logic. 03

(b) What is a macrooperation? Illustrate the sequence of microoperarions followed in macrooperation with an example. 04

(c) Explain the design of a simple computer with the help of block diagram. List various registers used in it. 07

Q.5 (a) Explain the term “active pull up”. 03

(b) Explain current hogging phenomenon in DCTL. 04

(c) Draw the circuit of 3 input TTL(Transistor Transistor Logic) NAND gate and explain its operation. 07

OR

Q.5 (a) State and define any three specifications of ADC. 03

(b) Draw the block diagram of Successive Approximation type ADC and explain its operation. 04

(c) With the help of neat diagram, explain the working of R-2R ladder type DAC. Draw suitable waveforms. 07

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