Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2132003 **Date: 02/06/2017**

Subject Name: Design Concepts in Basic Electronics

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	Explain the importance of self complimentary code with example.	
	2	In which complement system we have two 0?	
	3	What do you mean by the Gray code? What are its applications?	
	4	What are the logic levels used in TTL Logic system?	
	5	Explain don't care condition with proper example.	
	6	How does the look ahead carry adder speed up the addition process.	
	7	State excitation table and characteristics table for J K Flip Flop.	
	8	Why a filter circuit is required after rectifier?	
	9	Which are the two breakdown mechanisms in a P-N junction diode.	
	10	Define ripple factor.	
	11	Why CE configuration preferred over the other configuration	
	12	Explain the terms 1) A.C. Load line 2) D.C. load line	
	13	Explain thermal runaway.	
	14	What is voltage multipliers?	
Q.2	**(a)**	Explain the working of full wave doubler with help on neat diagram	**03**
	(b)	Show that both NAND and NOR gate are universal gate.	**04**
	(c)	A circuit receives a 4-bit excess-3 code. Design a minimal circuit to detect the decimal number 0,1,4,6,7,8.	**07**
		OR	
	(c)	Derive the following parameter for full wave bridge rectifier RMS load current, RMS load Voltage, Maximum efficiency, TUF, Ripple factor, Ripple frequency, DC load Power	**07**
Q.3	**(a)**	State the points of difference between combinational circuit and sequential circuit.	**03**
	(b)	Compare 1's and 2's complement method for doing substraction.	**04**
	(c)	Explain the effect of temperature on the V-I Characteristics of Diode	**07**
		OR	
Q.3	**(a)**	Explain setup time and hold time for edge triggered flip flop.	**03**
	(b)	Write down the tuth table for full adder and implement it with decoder.	**04**
	(c)	Explain the input output characteristic of n-p-n transistor in CE configuration. Also indicate different regions.	**07**
Q.4	**(a)**	Construct BCD to Excess-3 using 4-bit Binary Adder.	**03**
	(b)	Design the logic circuit that generate logic 1 if the 4-bit number is greater than 5 (0101)2 and implement using logic gates.	**04**
	(c)	Reduce the following Boolean expression using Quine-McCluskey (Tabulation) method and Implement with minimum number of NAND gates only. $F(A,B,C,D) = \sum_m (0,1,2,5,6,7,8,10,14,15)$	**07**

OR

Q.4	**(a)**	State the requirement of filter and explain any one filter circuit.	**03**
	(b)	State the use of clipping circuits and discuss with neat sketch working of a biased parallel clipper.	**04**
	(c)	Explain with neat diagram Voltage divider bias	**07**
Q.5	**(a)**	What are advantages of surface mount transistor.	**03**
	(b)	Which parameters related to time are important when transistor is used as a switch?	**04**
	(c)	Explain the input output characteristic of n-p-n transistor in CB configuration.Also indicate different regions.	**07**

OR

Q.5	**(a)**	Justify that current gain in common base configuration is less than and nearly equal to 1.	**03**
	(b)	What are factors affecting the stability of Q Point?	**04**
	(c)	Explain in detail fixed bias with its advantages and disadvantages.	**07**

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