Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2151007 **Date:10/05/2017**

Subject Name: Digital Design

Time:02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Do as Directed **[14]**

(1) What is entity?

(2) VHDL language is not technology-specific, but is capable of supporting technology-specific features. True or False?

(3) Entity name and architecture body may have same name. True or False?

(4) Write entity declaration for 1-bit full adder.

(5) State importance of package declaration.

(6) Difference between variable and signal.

(7) Give one example of subtype declarations.

(8) The order of values appearing in an enumeration type declaration defines the lexical order for the values. True or False?

(9) Process statement it self, a concurrent statement but all the statements written inside process statements are sequential statements. True or False?

(10) One entity may be assigned to many architecture bodies. True or False?

(11) List the 9 values of std_logic.

(12) What are purposes of Block statement?

(13) Difference between position association and named association.

(14) Every signal in a sensitivity list of a statement must change to fire the statement. True or False?

Q.2 (a) Explain CASE statement. **[03]**

(b) Differentiate between concurrent and sequential signal assignment statement. **[04]**

(c) Write brief note on VHDL data types. **[07]**

OR

(c) Explain various predefined operators in VHDL with their precedence. **[07]**

Q.3 (a) Explain Wait statement with example. **[03]**

(b) List the major capabilities of VHDL along with the features. **[04]**

(c) Explain modeling of MOOREY FSM with state diagram and code. **[07]**

OR

Q.3 (a) Differentiate between exit and next statements **[03]**

(b) What is difference between signal and variable with example? **[04]**

(c) What do you mean by Delta-delay? Also explain Inertial Delay model and Transport Delay model. **[07]**

Q.4 (a) Write VHDL Code for 4 X 1 DMUX using WITH/SELECT statement. **[03]**

(b) Write VHDL code for 2x4 decoder using dataflow modeling. **[04]**

(c) Explain modeling of MOOREY FSM with state diagram and code. **[07]**

OR

Q.4	**(a)**	Write VHDL Code for 1X 8 MUX using Case statement.	**[03]**
	(b)	Write VHDL code for 2x4 decoder using behavioral modeling.	**[04]**
	(c)	Explain modeling of MEALY FSM with state diagram and code.	**[07]**
Q.5	**(a)**	Explain CPLD Architecture in brief.	**[03]**
	(b)	Explain PLA with necessary Diagrams and equations.	**[04]**
	(c)	Draw and explain digital design flow for FPGA.	**[07]**

OR

Q.5	**(a)**	Compare PLA and ROM.	**[03]**
	(b)	Give the generic architecture for PLA, PAL	**[04]**
	(c)	What is FPGA? Draw its basic structure and give its applications.	**[07]**

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