Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2160909 **Date: 08/05/2017**

Subject Name: Advance Microcontrollers

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		**Short Questions**	**14**
	1	In STM32F4XX the main system consist of_____bit.	
	2	What is maximum internal AHB clock frequency?	
	3	What do you mean by NVIC in STM32F4XX?	
	4	SPI is a Synchronous_____Interface.	
	5	Bus arbitration available in which of the following protocol? (a) SPI (b) I2C	
	6	High speed output mode available in _____ timer.	
	7	In cortex M Processor ISA means_____.	
	8	During and just after reset, the I/O ports of STM32F4XX configured in output analog mode? True or false?	
	9	Thumb-2 Technology in Cortex-M processors _____ instructions? (a) Support only 16-bit (b) Support only 32-bit (c) Supports mixture of 16 bit & 32 bit	
	10	What is the function of GPIOx_MODER register?	
	11	All GPIO pin of STM32F4XX have weak pull-up and pull-down resistors, are activated or not depending on the value in the _____ register.	
	12	PWM mode in PCA timer can be activated by setting the bits of MATn and TOGn in CCAPMn register? True or False?	
	13	Basic timer (tim6&tim7) are 16-bit auto reload _____.	
	14	Which module of PCA timer can be programmed as watchdog timer?	
Q.2	**(a)**	Explain PCA module 4 as Watchdog timer.	**03**
	(b)	Explain the SPI control & SPI status registers in P89V51RD2.	**04**
	(c)	Using PCA timer in PWM mode, write 'C' code to generate wave of 75% duty cycle.	**07**
		OR	
	(c)	With the help of CMOD and CCON registers explain PCA timer.	**07**
Q.3	**(a)**	Draw master-slave SPI protocol and explain associated signals.	**03**
	(b)	Explain the PWM mode of PCA timer.	**04**
	(c)	Explain the I2C protocol in detail.	**07**
		OR	
Q.3	**(a)**	Explain the CCAPMn register in PCA timer of P89V51RD2.	**03**
	(b)	Draw PCA interrupt system of P89V51RD2.	**04**
	(c)	Explain the NVIC operation exception entry and exit of STM32F4XX.	**07**
Q.4	**(a)**	Discuss I-bus, D-bus and S-bus in STM32F4XX.	**03**
	(b)	Explain tail chaining in cortex M processors.	**04**
	(c)	Explain the comparison of round robin and round robin with interrupt software architecture in detail.	**07**

OR

Q.4	**(a)**	Compare Von Neumann and Harvard architecture.	**03**
	(b)	Explain multi-AHB bus matrix in STM32F4XX.	**04**
	(c)	Explain the bit banding technique in cortex M processors.	**07**
Q.5	**(a)**	Explain the main feature of TIM6 & TIM7 in STM32F4XX.	**03**
	(b)	Draw & explain the input configuration of GPIO in STM32F4XX.	**04**
	(c)	Explain the 3-stage pipelining in cortex CPU.	**07**

OR

Q.5	**(a)**	Explain the control registers of TIM6 & TIM7 in STM32F4XX.	**03**
	(b)	What do you mean by enumerator?	**04**
	(c)	Explain the feature of GPIO in detail.	**07**

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