Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2161004 **Date: 08/05/2017**

Subject Name: VLSI Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	Write full form of FPGA.	
	2	Define yield.	
	3	Define threshold voltage for MOSFET.	
	4	What is Body Effect?	
	5	Which type of MOSFET exhibits no current at zero gate voltage?	
	6	What are advantages of CMOS process?	
	7	Why NMOS technology is preferred more than PMOS technology?	
	8	Give name of different types of oxidation techniques.	
	9	When the channel is said to be pinched off?	
	10	What is punch through?	
	11	Define controllability.	
	12	Give any two examples of physical defects.	
	13	Write formula for the Elmore Delay.	
	14	High observability indicates that _____number of cycles are required to measure the output node value. (less/more)?	
Q.2	**(a)**	Define positive photoresist and negative photoresist.	**03**
	(b)	Explain the fabrication steps involved in LOCOS technique with suitable diagrams.	**04**
	(c)	Explain Y-chart of VLSI Design Flow.	**07**
		OR	
	(c)	Explain different packaging technology.	**07**
Q.3	**(a)**	Write I-V equation of N channel MOSFET for all regions.	**03**
	(b)	Explain channel length modulation.	**04**
	(c)	Calculate threshold voltage V_{T0} at room temperature for n-channel MOSFET, with following parameters: substrate doping density $N_A=10^{16}$ cm^{-3}, polysilicon gate doping density $N_D=2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox}=500Å and oxide interface fixed charge density $N_{ox}=4 \times 10^{10}$ cm^{-2}, $n_i=1.45 \times 10^{10}$ cm^{-3}, Φ_F (Gate) = -0.55 V, $\varepsilon_{ox} = 3.97\varepsilon_0$, $\varepsilon_{ox} = 11.7\varepsilon_0$, $\varepsilon_0=8.85\times10^{-14}$ F/cm.	**07**
		OR	
Q.3	**(a)**	Write I-V equation of P channel MOSFET for all regions.	**03**
	(b)	Explain constant field scaling.	**04**
	(c)	Write short note on MOSFET oxide related capacitance.	**07**
Q.4	**(a)**	Explain saturated enhancement load nMOS inverter.	**03**
	(b)	Explain CMOS ring oscillator circuit.	**04**
	(c)	Draw and explain voltage transfer characteristic of a realistic nMOS inverter.	**07**
		OR	

Q.4	**(a)**	Draw CMOS inverter and derive the expression for power delay product.	**03**
	(b)	Explain Noise Immunity and Noise Margins.	**04**
	(c)	Derive τ_{PHL} for CMOS inverter with necessary diagrams.	**07**
Q.5	**(a)**	Draw eight-transistor CMOS TG implementation and six-transistor CMOS TG implementation of 2 input XOR gate.	**03**
	(b)	Explain behavior of bistable element with two inverter circuit.	**04**
	(c)	Explain Built-in Self Test (BIST) techniques with necessary diagrams.	**07**
		OR	
Q.5	**(a)**	Draw and explain CMOS implementation of D-latch.	**03**
	(b)	Explain CPL NAND2 gate.	**04**
	(c)	Discuss ad-hoc testable design techniques.	**07**

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