Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2161101 **Date: 05/05/2017**

Subject Name: VLSI Technology & Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	When inversion is occurred in MOS system?	**01**
	2	Why channel is tapered in MOS transistor?	**01**
	3	Justify that constant drain current is flowing from MOS transistor in saturation region even though channel is pinched off.	**01**
	4	List out the types of capacitors available in CMOS inverter.	**01**
	5	Realize CMOS based D-flip flop circuit.	**01**
	6	Define : Subthreshold Current	**01**
	7	List out the function of Positive and Negative photoresists	**01**
	8	Define the term : Time to Market	**01**
	9	Define the terms : (1) Modularity (2) Locality	**01**
	10	Draw : Y- Chart for VLSI Design	**01**
	11	Draw the stick diagram for CMOS inverter	**01**
	12	Draw the layout of two input CMOS based NOR gate.	**01**
	13	List out the CAD tools available for VLSI design.	**01**
	14	Describe in brief : (1) ASIC design (2) System on Chip (SOC)	**01**
Q.2	**(a)**	List out advantages and disadvantages of pseudo PMOS transistor	**03**
	(b)	Justify that size of PMOS transistor chosen to be 2.5 times of an NMOS transistor.	**04**
	(c)	Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive the expressions of critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**07**
		OR	
	(c)	Discuss the resistive load inverter with the derivation of V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**07**
Q.3	**(a)**	Draw VLSI design flow with block diagram.	**03**
	(b)	Discuss the photolithography process used in fabrication of chip in brief.	**04**
	(c)	Explain two input depletion load NAND gate and derive the necessary equations for the same.	**07**
		OR	
Q.3	**(a)**	List out the fabrication steps of nMOS transistor with necessary figures.	**03**
	(b)	Derive the threshold voltage expression for MOSFET.	**04**
	(c)	Implement CMOS clocked RS fillip-flop.	**07**
Q.4	**(a)**	Realize XOR gate using CMOS transmission gate.	**03**
	(b)	Realize the following Boolean function using CMOS Transmission Gates. F = AB + A'C' + AB'C	**04**
	(c)	Implement and describe CMOS clocked JK latch.	**07**
		OR	
Q.4	**(a)**	Realize 2×1 Multiplexer using CMOS Transmission Gates.	**03**
	(b)	Implement the following Boolean function using CMOS. F = [(C+D+E) . (B+A)]'	**04**
	(c)	How will you calculate propagation delay times t_{pHL} and t_{pLH} for CMOS Inverter?	**07**
Q.5	**(a)**	List out possible electrical and logical faults observed in the circuit.	**03**

	(b)	Define controllability and observability with help of example.	**04**
	(c)	Explain the basic principles of pass transistor circuits. Also explain logic “0” and logic “1” transfer.	**07**

OR

Q.5	**(a)**	Differentiate between FPGA and CPLD	**03**
	(b)	Describe in brief : Built in Self Test (BIST)	**04**
	(c)	Draw the circuit diagram of Domino CMOS logic gate and discuss it in detail.	**07**

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