Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2161102 **Date: 03/05/2017**

Subject Name: Advanced Microprocessor

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		**Short Questions:**	**14**
	1	State the CISC design philosophy.	
	2	The code density is high for RISC processor. State true or false with justification.	
	3	Define Pipeline concept for any processor.	
	4	State the significance of conditional execution.	
	5	How many pipeline stages are there in ARM11 core?	
	6	State any two features of Berkeley RISC design rejected by ARM Architecture.	
	7	Which processor mode is nonprivileged in the case of ARM7TDMI core?	
	8	Operating system kernel operates in which mode of processor?	
	9	State the status of lower five bits of CPSR for Abort mode in the case of ARM7TDMI core.	
	10	State vector location of Software interrupt for ARM7TDMI.	
	11	Which flag is checked by ARM7TDMI core during the execution of conditional instruction having HS conditional attribute postfixed to the instruction mnemonic?	
	12	State the instruction used to come back the program sequence to the next instruction after the BL instruction is stored.	
	13	How much areas of virtual memory represent by all page tables except than master level page table?	
	14	How many levels of page table support by ARM MMU hardware?	
Q.2	**(a)**	List out in detail about any three designed rules implemented in RISC design Philosophy.	**03**
	(b)	Draw the ARM core dataflow model.	**04**
	(c)	Draw the structure of CPSR for ARM7TDMI core and also mention the function of control field.	**07**
		OR	
	(c)	Draw the diagram showing complete ARM register set or programmable register model for ARM7TDMI core and describe it in brief.	**07**
Q.3	**(a)**	Describe the nomenclature that ARM uses to describe the processor implementation.	**03**
	(b)	Draw the structure of the ARM cross-development toolkit.	**04**
	(c)	Describe the function performed by the following ARM mnemonics: (i) MVN (ii) RSB (iii) BIC (iv) TEQ (v) SMULL (vi) BL (vii) LDRSB	**07**

OR

Q.3	(a)	Describe the advantages of Thumb instructions by developing the division program using ARM instructions as well as Thumb instructions.	03
	(b)	Write an assembly language for ARM7TDMI core to swap the content of two register without using third register.	04
	(c)	Describe various addressing methods for stack operations for ARM architecture with the help of suitable LDM and STM mnemonics.	07
Q.4	(a)	Describe armcc and gcc compilers datatype mappings for ARM7TDMI core.	03
	(b)	Describe big endian configuration for various LDR and STR mnemonics.	04
	(c)	Develop C program to turn all eight LED connected with Port 0 Pin number 16 to 23 one by one from left to right and then right to left continuously. Assume that the anode of all the eight LED connected with port 0 pins and the cathode of all eight LED connected with ground through current limiting register.	07

OR

Q.4	(a)	Describe inline function and inline assembly and also state advantages of using it.	03
	(b)	Develop C program to read the status of the pull up switch connected with pin number of 16 of port 0 and display the LED connected with pin number 23 of port 0. The cathode of LED is connected with port 0 pin and the anode is connected with +5 V through resistor.	04
	(c)	Develop C program to display 00H to FFH continuously with delay between each count on two common anode seven segment display. Assume that the seven segment display on which D1 digit display is connected with the pin number 16 to 22 of Port 0 and the seven segment display on which D0 digit display is connected with the pin number 16 to 22 of Port 1.	07
Q.5	(a)	List out the steps requires to switch between tasks.	03
	(b)	Describe the steps or sequence of action performed by ARM processor core on the occurrence of any exception and interrupt.	04
	(c)	Describe how virtual memory works with the help of a diagram showing mapping a task in virtual memory to physical memory using a relocation register.	07

OR

Q.5	(a)	Describe any three ARM optimization techniques.	03
	(b)	Describe the components of a virtual memory system with the help of diagram.	04
	(c)	Describe AMBA arbitration with the help of diagram for a typical AMBA-based system.	07

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