Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII (NEW) - EXAMINATION – SUMMER 2017

Subject Code: 2172409 **Date: 06/05/2017**

Subject Name: Digital Signal Processing for Power Electronics

Time: 02.30 PM to 05.00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Do as directed : (02 marks each) **14**

(i) State equation for a backward difference system. Will it be causal?

(ii) Define IDFT. State its two applications.

(iii) Discuss significance of Nyquist rate for sampling.

(iv) For the signal shown in the Fig.1 .Evaluate the integral $\int_{-\pi}^{\pi} \left|X\left(e^{j\omega}\right)\right|^2 d\omega$.

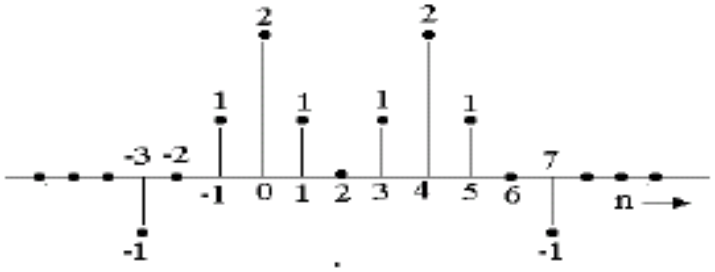

Fig.1

(v) What is overflow limit cycle? How it can be eliminated?

(vi) State relation between Fourier Transform & Z-Transform.

(vii) The figure shown Fig. 2 illustrates ……(Fill the blank).

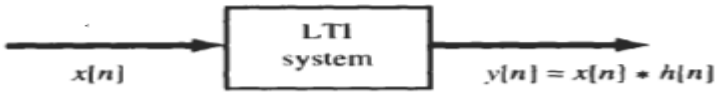

Fig.2

Q.2 **(a)** Consider a LTI system with system function as follows: **07**

$Z(s) = (1+2z^{-1} + z^{-2}) / (1 - 0.75 z^{-1} + 0.125 z^{-2})$.

Obtain (i) Direct form –I and (ii) Direct form –II structure.

Comments on the result obtained.

(b) Discuss cascade realization of FIR system in detail. **07**

OR

(b) Explain lattice structure realization for FIR system. **07**

Q.3 **(a)** Consider a causal system whose input and output satisfy the difference equation **06**

y(n)- a y(n-1) = x(n) .

(i) Find H(z) , ROC and condition(s) for stability.

(ii) Plot detailed pole-zero diagram.

(iii) Given system is IIR or FIR? Why?

	(b)	State and prove the following properties of DFT: (i) linearity (ii) duality (iii) periodicity (iv) circular convolution.	**08**
		OR	
Q.3	**(a)**	For the T {x(n) } = a x(n) + b system with a > 0 & b > 0, determine whether the system is (i) stable (ii) causal (iii) linear (iv) time –invariant (v) memory less. (vi) If b = 0, what will be effect on linearity? (vii) If a=0, what will be effect on causality?	**06**
	(b)	Find the 4- point DFT of the sequence x(n) ={1,1,0,0}.	**08**
Q.4	**(a)**	Explain DIT- FFT algorithm using signal flow graphs for N= 4.	**07**
	(b)	Draw and explain the block diagram of basic generic hardware architecture for a digital signal processor.	**07**
		OR	
Q.4	**(a)**	What is truncation? Sketch the characteristics of (i) Two's complement quantizer & (ii) one's complement quantizer.	**07**
	(b)	Draw and explain the block diagram of architecture for modified Harvard digital signal processor.	**07**
Q.5	**(a)**	What are the different formats of fixed point representation? Explain the fixed point representation of binary numbers.	**07**
	(b)	How reduction in product round off errors is achieved?	**07**
		OR	
Q.5	**(a)**	Discuss the concept of zero input limit cycle oscillation. How this can be eliminated?	**07**
	(b)	Compare fixed point and floating point representation. State any one IEEE format to represent a 32 bit floating point number.	**07**

****