GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–III • EXAMINATION – SUMMER 2013

Subject Code: 130701   **Date: 27-05-2013**
Subject Name: Digital Logic Design
Time: 02.30 pm - 05.00 pm   **Total Marks: 70**

Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Convert the decimal number 250.5 to base 3, base 4, base 7and base 16.	**07**
	(b)	Perform the subtraction with the following decimal numbers using 1∅s compliment and 2∅s compliments. (a) 11010-1101 , (b) 10010-10011	**07**
Q.2	**(a)**	Simplify the following Boolean functions to a minimum numbers of literals. (a) xyz+x∅y+xyz∅ and (b)(A+B)∅(A∅+B∅)∅	**07**
	(b)	Obtain the truth table of the function F= xy+xy∅+y∅z	**07**
		OR	
	(b)	Implement the Boolean functions.	**07**
Q.3	**(a)**	Implement the Boolean functions.(a) xyz+x∅y+xyz∅ (b) (A+B)∅(A∅+B∅)∅ and (c) F= xy+xy∅+y∅z with logic gates.	**07**
	(b)	Show that the dual of the exclusive-OR is equal to its compliment.	**07**
		OR	
Q.3	**(a)**	Obtain the simplified expression in sum of product for the following Boolean functions. (a) F= Û(0,1,4,5,10,11,12,14) and (b) F= Σ(11,12,13,14,15).	**07**
	(b)	Implement the functions F= Σ(1,3,7,11,15) with don∅t care conditions d= Σ (0,2,5) Discuss the effect of don∅t care conditions.	**07**
Q.4	**(a)**	Explain half and full adders in detail.	**07**
	(b)	Design and implement BCD to excess 3 code converter.	**07**
		OR	
Q.4	**(a)**	What is the difference between serial and parallel transfer? What type of registers are used in each case?	**07**
	(b)	Design a synchronous BCD counter with JK flip flops.	**07**
Q.5	**(a)**	Explain a 4 to 1 line multiplexer in detail.	**07**
	(b)	Explain PLA in detail.	**07**
		OR	
Q.5	**(a)**	Explain scratchpad memory in detail.	**07**
	(b)	Explain D type positive edge triggered flip flop.	**07**

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