Seat No.: _____   Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–V • EXAMINATION – SUMMER 2013

Subject Code: 150701   **Date: 14-05-2013**
Subject Name: Advance Processors
Time: 10.30 am - 01.00 pm   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following questions   **07**
       1. What is pipelining?
       2. If the stack segment register contains 3000H and the stack pointer register contains 2400H.What is the physical address of the top of the stack?
       3. What is the use of direction flag in 8086? Which instruction is used to set direction flag?
       4. What is the difference between RET and IRET instructions?
       5. How does 8086 respond to INTO instruction?
       6. Explain wait instruction of 8086
       7. What is the maximum amount of virtual memory possible with 80386?
       8. Justify your answer

(b) Briefly explain following directives with example: **03**
1. EVEN , DW , PTR   **2. AAA , MUL, LOOPE and CBW**   **04**

Q.2 **(a)** Write a near procedure which multiplies two 8 bit numbers. Write a main program which use above procedure two multiply two 16 bit numbers.   **07**

(b) What are the differences between near and far procedure? Briefly explain four parameter passing methods with their advantages and disadvantages.   **07**

OR

(b) Write an 8086 assembly program which unpacked two digits from a packed BCD byte and find seven segment codes of both the digits. Send seven segment codes on output ports with address FF00H and FF02H respectively.   **07**

Q.3 **(a)** Briefly explain priority structure of interrupts in 8086. Suppose 8086 receive low to high transition on NMI input during execution of DIV instruction and that division operation produces a divide by zero error. How does 8086 responds?   **07**

(b) What are the differences between minimum mode and maximum mode operation of 8086? Draw minimum mode system with RAM, ROM and I/O port.   **07**

OR

Q.3 **(a)** Explain respond of 8086 when it executes instruction INT 10H.Also explain respond of 8086 when it receive signal on INTR.   **07**

(b) Draw and explain memory read machine cycle of 8086 in minimum mode. Briefly explain ODD and EVEN bank concept in 8086.   **07**

Q.4 **(a)** Explain four function units of 80286.Also explain MMU of 80286.   **07**

(b) Briefly explain address pipelining concepts in 80386.Explain two mechanisms used to protect I/O in protected mode of 80386.   **07**

OR

Q.4 **(a)** Explain segment descriptor and call gate descriptor in 80386.Breifly explain use of call gate descriptor   **07**

Q.4 **(b)** Explain task state segment (TSS) and task register (TR) in 80386. Briefly explain different ways of task switching in 80386.   **07**

Q.5 **(a)** Compare real mode, protected mode and virtual 8086 mode in 80386.Briefly **07** explain interrupt handling in Protected mode.

(b) Briefly explain six function units of 80486 and discuss new features in 80486 **07** compared to 80386.

OR

Q.5 **(a)** Briefly explain superscalar architecture, Hyper thread technology and core 2 duo **07** technology in Intel P6 family processor

(b) Compare CISC and RISC architecture. Briefly explain Register window in **07** SUNSPARC.

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