Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI • EXAMINATION – SUMMER 2013

Subject Code: 161004 Date: 03-06-2013

Subject Name: VLSI Technology and Design

Time: 10.30 am - 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Briefly discuss following: **07**

1. Observability in testing
2. Write the Current-Voltage equations of the n-channel MOSFETS.
3. Need of Domino CMOS logic
4. Modularity in VLSI design
5. Noise Margin High
6. Channel Length Modulation
7. Advantages of NORA CMOS logic circuits

(b) Discuss VLSI Design flow in detail. **07**

Q.2 **(a)** Discuss MOSFET capacitances in brief. **07**

(b) Derive expression for propagation delay times τ_{PHL} and $\tau_{PLH.}$ **07**

OR

(b) Draw circuit for CMOS two input NOR gate. Derive V_{TH} of the same. **07**

Q.3 **(a)** Draw the Resistive Load Inverter circuit. Derive critical voltage points VOH,VOL,VIL and VIH for Resistive Load Inverter circuit. **07**

(b) Consider a resistive-load inverter circuit with VDD =5 V, Knô =10ε A/V^2 , VTO=0.8V, RL=200kq ,and W/L=4.Calculate the critical Voltages (V_{OH},V_{OL},V_{IL} & V_{IH}) on the VTC and find the noise margins of the circuit. **07**

OR

Q.3 **(a)** Explain Band Diagram of the MOS structure, at surface Inversion. Derive the expression of threshold Voltage. **07**

(b) What is the need of Scaling? Discuss constant voltage scaling in detail with its merits and demerits. **07**

Q.4 **(a)** Discuss CMOS transmission gate for all operating regions and plot equivalent resistance of CMOS transmission gate as a function of output voltage. **07**

(b) Discuss Master Slave Flip-Flop in brief. **07**

OR

Q.4 **(a)** Explain the basic principles of pass transistor circuits. Also explain logic ñ0ò and logic ñ1ò transfer. **07**

(b) Discus Voltage Bootstrapping. **07**

Q.5 **(a)** Explain On Chip Clock Generation and Distribution. **07**

(b) Discuss following: **07**

1. Basic steps of the Local Oxidation of silicon(LOCOS) process to create oxide isolation around active areas.
2. Prevention of Latch-up

OR

Q.5 **(a)** Discuss Built-in Self Test (BIST) techniques **07**

(b) Discuss following: **07**

(1) List VLSI design styles and discuss FPGA

(2) Compare Enhancement MOSFET and Depletion MOSFET

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