Seat No.:	Enrolment No.
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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III • EXAMINATION – SUMMER • 2014

Subject Code: 130704 Date: 23-05-2014 Subject Name: Computer Organization and Architecture Time: 02.30 pm - 05.00 pm Total Marks: 70		Code: 130704 Date: 23-05-2014	
	ruction	<u> </u>	
	1.	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks.	
Q.1	(a) (b)	Design and Explain Common bus system using multiplexer. Draw and explain the flowchart for instruction cycle.	07 07
Q.2	(a) (b)	Explain Design of Control Unit. Draw and explain first pass assembler. OR	07 07
	(b)	Explain the working of Second Pass Assembler with its flowchart and its importance.	07
Q.3	(a) (b)	Explain input-output instructions. Write short note on subroutines.	07 07
		OR	
Q.3	(a) (b)	Explain Memory reference instructions. Explain various types of interrupts.	07 07
Q.4	(a)	Define Following Terms: 1) Computer Organization 2) Computer Architecture 3) Accumulator 4) Hardwired control 5) Register Transfer Language 6) Pseudo instructions 7) Micro operation	07
	(b)	Write an assembly language program to Add two double precision numbers. OR	07
Q.4	(a)	Explain the following instructions: BUN, ISZ, CLA, CLE, CIR, SPA, SKI.	07
	(b)	Write an assembly language program to multiply two positive numbers.	07
Q.5	(a) (b)	Explain booth algorithm for multiplication with a flowchart. Explain the Instruction Pipelining with example. OR	07 07
Q.5	(a) (b)	Multiply the (-9) with (-13) using Booth's algorithm. Give each step. Considering three segment instruction pipeline, illustrate the concepts of delayed load and delayed branch with example.	07 07
