## **GUJARAT TECHNOLOGICAL UNIVERSITY** BE - SEMESTER-V • EXAMINATION – SUMMER • 2014

Subject Code: 150701 Date: 11-06-20			
Sul Tir Inst	bject ne: 10 ruction	Name: Advance Processors0.30 am - 01.00 pmTotal Marks: 70ns:	
	1. 2. 3.	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks.	
Q.1	(a)	<ul> <li>(1) What are the steps taken by 8086 when interrupt comes?</li> <li>(2) How does 8086 architecture make the instruction fetching and instruction execution independent using prefetch queue? Explain</li> </ul>	07
	<b>(b)</b>	Explain the addressing modes of 8086 with example	07
Q.2	(a)	Draw and explain 8086 pin diagram	07
	<b>(b</b> )	Explain 8086 interrupt vector table. OR	07
	<b>(b)</b>	Draw and explain 8086 internal block diagram	07
Q.3	(a)	List and explain the various Bit Manipulation and String instructions with examples.	07
	<b>(b)</b>	Describe MMX and Hyper Threading.	07
03	<b>(</b> 2 <b>)</b>	Differentiate between CISC and RISC	07
Q.S	( <b>b</b> )	Discuss Minimum mode operation of 8086	07 07
Q.4	(a)	List three major advances that the 80386 microprocessor has over the 80286. Draw and explain how a 32-bit virtual address for a data segment location in a task's local memory is translated to the actual 32-bit physical address for a 386 operating in segments only protected mode.	07
	(b)	Draw a flow chart or write the pseudocode and then write an 8086 assembly language program for adding a constant to a series of values in memory. OR	07
Q.4	(a)	Draw and explain pin diagram of 80286 microprocessor. Also explain 80286 protected-mode operation.	07
	(b)	Draw a flow chart or write the pseudocode and then write an 8086 assembly language program for finding the average of any number of bytes in an array in memory. The number of bytes to be added is in the first byte of the array.	07
Q.5	<b>(a)</b>	Draw and explain Intel 486 internal block diagram	07
	(b)	What is macro? How can you define and call macros? Give an example of macro with parameter.	07
05	(z)	OR Describe Decentrant and Decentric procedures	07
Q.5	(a) (b)	Explain the architecture of SUN SPARC processor.	07 07

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