Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII • EXAMINATION – SUMMER 2014

Subject Code: 180802 **Date: 31-05-2014**

Subject Name: VLSI Technologies

Time: 10:30 am TO 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q-1	**(a)**	Explain VLSI Design flow using Y-chart.	**07**
	(b)	Explain the fabrication steps of nMOS transistor with necessary figures.	**07**
Q-2	**(a)**	Draw the CMOS Inverter circuit and VTC for different operation regions of the nMOS and pMOS transistor. Derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**07**
	(b)	An enhancement nMOS transistor has the following parameters: Threshold voltage Vth=0.8v, channel length modulation coefficient $\lambda=0.05V^{-1}$, Process transcounductance parameter $\mu_n Cox = 20A/V^2$. If the transistor is biased with V_G = 2.8V, V_D = 5V and V_S= 1V. The drain current is say I_D=0.24mA. Determine W/L.	**07**
		OR	
	(b)	Design a CMOS logic gate for the function. $f = \overline{ab+ac+bd}$ using smallest number of transistors.	**07**
Q-3	**(a)**	Explain energy band diagram of MOS structure at surface inversion and derive the equation of threshold voltage.	**07**
	(b)	Derive the expression for drain current as a function of V_{GS}, V_{DS} and V_{SB} for all three region of operation of MOSFET using Gradual Channel Approximation.	**07**
		OR	
Q-3	**(a)**	How will you calculate propagation delay times τ_{pHL} and τ_{pLH} for CMOS Inverter?	**07**
	(b)	Explain Voltage Bootstrapping.	**07**
Q-4	**(a)**	Explain the functioning of depletion load nMOS inverter and derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**07**
	(b)	Explain two input depletion load NOR gate and derive the necessary equations for the same.	**07**
		OR	
Q-4	**(a)**	Explain the basic principle of pass transistor circuit. Explain logic “1” transfer and logic “0” transfer.	**07**
	(b)	Draw the circuit diagram of Domino CMOS logic gate and discuss it in detail.	**07**
Q-5	**(a)**	Discuss basic steps of the LOCOS Process.	**07**
	(b)	Concept of regularity, modularity and locality	**07**
		OR	
Q-5	**(a)**	Write a short note on Built In Self Test (BIST).	**07**
	(b)	Give comparison between FPGA and CPLD.	**07**

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