Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– VI• EXAMINATION–SUMMER 2015

Subject Code: 161004 **Date:14/05/2015**

Subject Name: VLSI Technology and Design

Time: 10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as Directed: **07**

1. Draw Voltage Transfer Characteristics of Enhancement mode and Depletion mode MOSFETs.
2. Is PMOS is subjected to substrate-bias effect (Body effect) in CMOS Inverter? Justify your answer.
3. Briefly describe yield and manufacturability.
4. Define Positive photoresist and negative photoresist.
5. As we reduce V_{DD} of CMOS inverter, write $V_{DD\ (Min)}$ for which CMOS inverter operates correctly?
6. Draw general layout of an H-tree clock distribution network.
7. Discuss controllability in brief.

(b) Discuss MOSFET capacitances in brief. **07**

Q.2 **(a)** Discuss guideline for avoiding of CMOS Latch-Up. **07**

(b) Derive the expression for τPHL for CMOS Inverter for ideal step as an input to CMOS Inverter. **07**

OR

(b) Discuss VLSI Design flow in detail. **07**

Q.3 **(a)** Draw the CMOS Inverter circuit and Voltage Transfer Characteristic (VTC) for different operating regions of the nMOS and pMOS transistors. Derive critical voltage points V_{OH},V_{OL},V_{IL} , V_{IH} . **07**

(b) Consider a CMOS Inverter circuit with the following parameters: **07**
V_{DD}=3.3V, $V_{TO,n}$=0.6V , $V_{TO,p}$= - 0.7V, k_n=400 microAmp/V^2, k_p=160 microAmp/V^2 .
Calculate the noise margin of the circuit.

OR

Q.3 **(a)** Draw the Inverter circuit with Resistive Load Inverter. Derive critical voltage points VOH, VOL, VIL and VIH for Resistive Load Inverter circuit. **07**

(b) Consider a resistive-load inverter circuit with VDD =5 V, Kn' =10 MicroA/V^2 , VTO=0.8V, RL=400kΩ,and W/L=2.Calculate the critical Voltages (VOH,VOL,VIL and VIH) on the VTC and find the noise margins of the circuit. **07**

Q.4 **(a)** Draw the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region. **07**

(b) Derive Req of all regions in CMOS Transmission gates and draw a graph of equivalent R plotted as a function of output voltage. **07**

OR

Q.4 **(a)** Discuss CMOS SR latch circuits based on NOR2 gates. **07**

(b) Discuss Ad hoc testable design techniques. **07**

Q.5 **(a)** Discuss basic principles of Pass transistor circuits and Logic "1" transfer. **07**

(b) Explain domino CMOS logic. **07**

OR

Q.5 **(a)** Describe the process of fabrication of the NMOS transistor. **07**

(b) Explain Built-in Self Test (BIST) techniques with necessary diagrams. **07**

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