Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–VIII • EXAMINATION – SUMMER • 2015

Subject code: 180802 **Date : 11/05/2015**

Subject Name: VLSI Technologies

Time : 10.30AM-01.00PM **Total marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q-1	**(a)**	Draw and explain y chart in detail.	**7**
	(b)	Explain design procedure steps for fabrications of p-MOS transistor.	**7**
Q-2	**(a)**	Explain Channel Length Modulation	**7**
	(b)	Draw and explain the structure of MOSFET transistor. Derive the expression for Threshold of MOSFET transistor.	**7**
		OR	
Q-2	**(b)**	What kind of approximation is used to establish MOSFET voltage current relationship? With the help of that derive the expression which gives the relation between input voltage (Vgs) and current (Id)	**7**
Q-3	**(a)**	Draw the CMOS inverter circuit and VTC for different operating regions of the nMOS and PMOS transistor. Derive VOH,VOL,VIH and VIL.	**7**
	(b)	Explain Device Isolation Technique and Locos.	**7**
		OR	
Q-3	**(a)**	Give the delay time definitions and calculation of delay times.	**7**
	(b)	Write a short note on MOSFET Capacitance.	**7**
Q-4	**(a)**	Concept of regularity, modularity and locality.	**7**
	(b)	Write a short note on FPGA.	**7**
		OR	
Q-4	**(a)**	Explain Gradual Channel Approximation of MOSFET.	**7**
	(b)	Explain the MOS system under external bias.	**7**
Q-5	**(a)**	Explain two input depletion load NOR gate and derive the necessary equations for the same.	**7**
	(b)	Explain the basic principle of pass transistor circuit. Explain logic “1” transfer and logic “0” transfer.	**7**
		OR	
Q-5	**(a)**	Explain Depletion Load nMOS inverter	**7**
	(b)	Write a short note on Built In Self Test (BIST).	**7**
