Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (NEW)EXAMINATION – SUMMER 2015

Subject Code: 2130306 **Date:04/06/2015**

Subject Name: Fundamentals of Digital Design

Time: 02.30pm-05.00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define following parameters. I) Fan-out, II) Propagation delay, III) maxterm and minterm , IV) combinational circuit, V) sequential circuit ,VI) Flip-flop VII) noise margin	**07**
	(b)	Explain moore and Mealy model of sequential circuit.	**07**
Q.2	**(a)**	Design combinational circuit for binary to octal conversion.	**07**
	(b)	Explain BCD Ripple counter and draw its logic diagram and timing diagram.	**07**
		OR	
	(b)	Explain 4 bit Magnitude Comparator.	**07**
Q.3	**(a)**	Derive Boolean function using Tabulation Method for the following: F(A,B,C,D) = ∑(0,1,3,4,5,7,10,13,14,15)	**07**
	(b)	Design a 4x16 decoder with two 3x8 decoders.	**07**
		OR	
Q.3	**(a)**	Design a sequential circuit using JK Flip-Flops and two states Q0 and Q1 such that , 1. It moves to the next state for input 0. (00 to 01, 01 to 10,…, 11 to 00) 2. It moves to the previous state for input 1. (reverse from the above mentioned steps)	**07**
	(b)	Explain FPGA and CPLD in detail.	**07**
Q.4	**(a)**	Show how a full-adder can be converted to a full-subtractor with the addition of one inverter circuit.	**07**
	(b)	Design 8 * 1 multiplexer for given function F(A,B,C,D) = ∑(0,1,3,4,5,7,10,13,14,15).	**07**
		OR	
Q.4	**(a)**	Convert the Decimal Number 250.5 to base 3, base 4, base 7 & base 16.	**07**
	(b)	Simplify the Boolean Function with Karnaugh map: (i) F(w,x,y,z) = Σ(0,1,2,4,5,6,8,9,12,13,14) and (ii) F = A´B´C´+B´CD´+A´BCD´+AB´C´	**07**
Q.5	**(a)**	Explain in brief: Programmable Logic Array	**07**
	(b)	Write a note on Master-Slave J-K Flip-Flop.	**07**
		OR	
Q.5	**(a)**	Draw circuit of two inputs TTL NAND GATE. Explain its working. Compare it with RTL in terms of speed and power consumption with reasoning.	**07**
	(b)	Explain Dual slope A/D converter.	**07**

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