Seat No.: _____ Enrollment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER-III (NEW) • EXAMINATION – SUMMER-2015

Subject Code: 2132003 **Date:27/05/2015**

Subject Name: Design Concepts in Basic Electronics

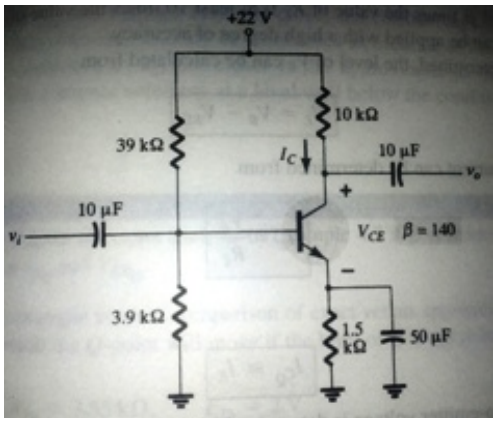
Time:02.30pm-05.00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	1) Answer the following question. i) Define Digital System. ii) Convert $(2C6B.F2)_{16}$ into its equivalent Binary. iii) Convert $(8)_{10}$ into equivalent BCD and Excess-3 code. iv) Convert $(414)_8$ into its equivalent Hexadecimal and Binary.	**04**
		2) Comparison between 1's and 2's compliments.	**03**
	(b)	Explain Digital Logic Gates with Symbol, Algebraic function and Truth Table.	**07**
Q.2	**(a)**	1) State the truth table of full-adder and half-adder.	**03**
		2) Draw the logic diagram and state truth table of 4x1 multiplexer.	**04**
	(b)	Draw and Explain the working of clocked RS flip-flop.	**07**
		OR	
	(b)	Draw and Explain the working of JK flip-flop.	**07**
Q.3	**(a)**	Design 4-bit up-down binary counter with the help of T flip-flop.	**07**
	(b)	Define term Register. Define the 'Different Modes of Operation' of Register.	**07**
		OR	
Q.3	**(a)**	With the logic diagram explain the operation of 4-bit binary ripple counter.	**07**
	(b)	Explain with neat diagram working of 4-bit bidirectional shift register with parallel load.	**07**
Q.4	**(a)**	Explain Forward Bias and Reverse Bias.	**07**
	(b)	Give the points of difference between Half wave, Full wave and Bridge Rectifier.	**07**
		OR	
Q.4	**(a)**	Explain in detail different types of breakdown in diode.	**07**
	(b)	Explain different configuration of clippers.	**07**
Q.5	**(a)**	Explain the input output characteristics of n-p-n transistor in Common-Collector configuration.	**07**
	(b)	Draw fixed-bias circuit and explain Collector-Emitter loop.	**07**
		OR	
Q.5	**(a)**	Explain the input output characteristics of p-n-p transistor in Common-Emitter configuration.	**07**

(b) Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of fig. **07**



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