Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(OLD) • EXAMINATION – WINTER 2016

Subject Code:130701 **Date:02/01/2017**

Subject Name:Digital Logic Design

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as directed. **07**

(1) $(645.65625)_{10} = (\quad)_2$ (5) $(ABC.555)_{16} = (\quad)_8$

(2) $(FACE.25)_{16} = (\quad)_{10}$ (6) $(2493)_{10} = (\quad)$Excess-3 Code

(3) $(11011)_{Gray} = (\quad)_{10}$ (7) $(1525)_{10} = (\quad)_{Gray\ Code}$

(4) Subtract $(45)_{10}$ from $(93)_{10}$ _using 1's complement method.

(b) Explain with neat logic diagram and truth table the functioning of basic logic gates. **07**

Q.2 **(a)** Minimize the following function using K-map and implement the same. **07**

F (w,x,y,z) = ∑m (0,1,2,3,6,7,13,14) + ∑d (8,9,10,12)

(b) Minimize the following function using K-map and implement the same. **07**

F = A'B'C' +B'CD' + A'BCD' + AB'C'

OR

(b) Justify the statement: "NAND and NOR gates are universal gates." **07**

Q.3 **(a)** Design and explain BCD Counter. **07**

(b) With neat logic diagram, explain serial in parallel out shift register. **07**

OR

Q.3 **(a)** Design and explain with truth table the logic circuit for full adder. **07**

(b) Design and explain Odd parity generator. **07**

Q.4 **(a)** Draw & explain Master-Slave J-K Flip Flop. **07**

(b) Explain Arithmetic, Logic and Shift Micro operations in detail. **07**

OR

Q.4 **(a)** Draw & explain T Flip Flop and D Flip Flop. **07**

(b) Design and explain 3 to 8 line Decoder. **07**

Q.5 **(a)** Write a short note on Micro Program Control. **07**

(b) Design and explain 4x1 Multiplexer. **07**

OR

Q.5 **(a)** Write a short note on Hard-Wire Control. **07**

(b) Explain in detail Inter-register Transfer logic. **07**

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