Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) • EXAMINATION – WINTER 2016

Subject Code:2130306 **Date:09/01/2017**

Subject Name:Fundamentals of Digital Design

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	$(1234)_{10} = (\ )_{16}$	
	2	$(EB.CD)_{16} = (\ )_{8}$	
	3	$(125.25)_{10} = (\ )_{2}$	
	4	$(101110.01)_{2} = (\ )_{10}$	
	5	What is HDL & VHDL?	
	6	What is difference between binary code and BCD code?	
	7	$1101 \times 1010 = (\ )_{2}$	
	8	What is difference between binary code and gray code?	
	9	Draw symbol & truth table of D-flip flop.	
	10	Define Noise margin.	
	11	Define Propagation delay.	
	12	Define Fan out.	
	13	Discuss resolution of D/A convertor.	
	14	Give the difference between combinational & sequential circuit.	
Q.2	**(a)**	Perform (-7) – (-3) using 2's complement method.	**03**
	(b)	State and prove De Morgan's Theorems with the help of truth tables.	**04**
	(c)	Prove universality of NAND & NOR gate.	**07**
		OR	
	(c)	Explain basic theorems of Boolean algebra with example.	**07**
Q.3	**(a)**	Design & explain full subtractor.	**03**
	(b)	Simplify the function using K-map. Y = ∑m(0,1,5,9,13,14,15) + d(3,4,7,10,11).	**04**
	(c)	Implement the function $F = (\bar{A} + B\bar{C})(CD + \bar{E})$ using NAND gates.	**07**
		OR	
Q.3	**(a)**	Design full adder circuit using half adder.	**03**
	(b)	Simplify the function using K-map. Y = ∑m(1,3,5,6,10,13,15) & draw logic diagram.	**04**
	(c)	Determine the prime implicants of the following function using tabulation method: F(W, X, Y, Z) = Σ(1, 4, 6, 7, 8, 9, 10, 11, 15).	**07**
Q.4	**(a)**	Give the classification of logic devices.	**03**
	(b)	Explain operation of 8:1 multiplexer with truth table & logic diagram.	**04**
	(c)	Design 4-bit binary to BCD code convertor.	**07**
		OR	

Q.4	**(a)**	Explain the types of ROMs.	**03**
	(b)	With logic diagram & truth table explain the working of 3 to 8 line decoder.	**04**
	(c)	Design a combinational circuit whose input is 3-bit number & output is seven segment code of input number.	**07**
Q.5	**(a)**	What is race-around condition in JK flip-flop? How can we avoid it?	**03**
	(b)	Explain PAL in detail with necessary diagram.	**04**
	(c)	Design Mod 10 Counter using J-K Flip flop.	**07**

OR

Q.5	**(a)**	Compare PLA and PROM.	**03**
	(b)	Explain successive approximation type ADC.	**04**
	(c)	Explain Moore & Mealy model for sequential circuit.	**07**

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