Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) • EXAMINATION – WINTER 2016

Subject Code:2131704 **Date:06/01/2017**

Subject Name:Digital Logic Circuits

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Short questions:	14
	1	Perform the following binary subtraction using 2's complement method: $(110000-10111)_2$	1
	2	Convert the given octal number to equivalent hexadecimal number: $(247.36)_8$	1
	3	What do you mean by the term "Standard Canonical form"?	1
	4	What is meant by positive logic and negative logic?	1
	5	Which is the fastest logic family? Why?	1
	6	Which one of the following is more accurate DAC? Why? I) Weighted resistor type DAC II) R-2R ladder type DAC	1
	7	Define the term Propagation delay with respect to digital logic families.	1
	8	What is excitation table?	1
	9	What is the difference between combinational circuit and sequential circuit?	1
	10	Ripple counters are _____ counters. I) Asynchronous II) Synchronous	1
	11	What is overflow condition in registers?	1
	12	Define the term "resolution" with respect to ADCs.	1
	13	What is reflected code?	1
	14	Define the term " Modulus of the counter"	1
Q.2	(a)	What is race around condition? How can it be resolved?	3
	(b)	Draw the diagram of Switched capacitor type DAC and explain its operation.	4
	(c)	Explain the working of Flash type A/D converter.	7
		OR	
	(c)	Explain the working of Dual slope type A/D converter.	7
Q.3	(a)	Implement a full adder circuit with a decoder and two OR gates.	3
	(b)	Simplify the following equation using K-map and implement using logic gates: $F(A,B,C,D) = \sum(0,1,2,3,5,7,8,9,11,14)$	4
	(c)	Simplify the following equation using tabulation method: $F(W, X, Y, Z) = \sum(0,1,2,8,10,11,14,15)$	7
		OR	
Q.3	(a)	Design BCD to Decimal decoder using K- map.	3
	(b)	Simplify the following equation using K-map and implement using universal gates: $F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$	4
	(c)	Design gray code to binary code converter using K-map.	7
Q.4	(a)	Write a short note on PLA.	3
	(b)	Implement the following function with 8:1 multiplexer: $F(A, B, C, D)= \sum(0, 1, 3, 4, 8, 9, 15)$	4
	(c)	Draw the block diagram of BCD adder and explain the logic of BCD addition in it.	7
		OR	
Q.4	(a)	Explain different types of triggering methods.	3

(b) Draw the logical diagram of Jhonson counter and explain its operation. 4

(c) Design a counter that has a repeated sequence of six states as given below: 7

A	B	C
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

Q.5 (a) Draw CMOS NAND gate and justify the output for various input states. 3

(b) Explain Totem pole output in TTL logic. 4

(c) Draw the circuit of ECL OR-NOR gate and explain its operation. 7

OR

Q.5 (a) Explain the working of 4:1 multiplexer. 3

(b) Explain ALU. 4

(c) Explain arithmetic, logic and shift micro operations 7