Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) • EXAMINATION – WINTER 2016

Subject Code:2132003 Date:04/01/2017

Subject Name:Design Concepts in Basic Electronics

Time:10:30 AM to 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Answer the following questions to the point:	**07**
	1.	Convert 11011.101_2 to decimal base.	
	2.	$\sqrt{(41)} = 5$ is a valid computation in which base system?	
	3.	Differentiate between Binary and BCD codes.	
	4.	How does a Gray code perform better than a Binary code?	
	5.	Draw the symbol of a JK FF and state its truth table.	
	6.	Which FF is used to form different types of shift registers?	
	7.	What is the drawback of a ripple counter?	
	(b)	Answer the following questions to the point:	**07**
	1.	Draw the common emitter configuration using an npn transistor	
	2.	Of all the biasing methods available for a transistor, which is the best? Why?	
	3.	What is the significance of the slope of a load line?	
	4.	"Q point is defined as the point of intersection of the load line with the output characteristics of the device." Justify.	
	5.	What is the location of the Q point for cutoff operation?	
	6.	What is the value of collector current for saturated region of operation?	
	7.	State the parameters on which the value of current gain depends.	
Q.2	**(a)**	Implement an X-OR gate using NAND gates only.	**03**
	(b)	State and prove De- Morgan's theorems.	**04**
	(c)	Solve $f(A,B,C,D)= \Pi M(4,7,10,11,12,15).d(6,14)$. Draw AOI logic.	**07**
		----------OR----------	
Q.2	**(a)**	Implement an X-NOR gate using NOR gates only.	**03**
	(b)	Subtract 6 from 10 in binary using 1's & 2's complement methods.	**04**
	(c)	Solve $f(A,B,C,D)= \sum m(0,2,6,10,11,12,13)+d(3,4,5,14,15)$. Draw AOI logic.	**07**
Q.3	**(a)**	How does a combinational circuit differ from sequential circuit?	**03**
	(b)	Explain the working of a master slave JK FF.	**04**
	(c)	Explain the working of a 3 to 8 decoder circuit. Implement a Full Adder circuit using the same.	**07**
		----------OR----------	
Q.3	**(a)**	Differentiate between synchronous and asynchronous sequential circuits.	**03**
	(b)	Define propagation delay, fan in, power dissipation and noise margin.	**04**
	(c)	Draw an 8X1 multiplexer circuit. Implement a 16X1 multiplexer using 4X1 multiplexer and combination logic if needed.	**07**
Q.4	**(a)**	Define all types of shift register? Explain the working of any one of them.	**03**
	(b)	Explain the working of a 3 bit ripple down counter.	**04**
	(c)	Explain the working of a positive and negative clamper circuit.	**07**
		----------OR----------	
Q.4	**(a)**	Explain the working of a BCD synchronous up counter.	**03**
	(b)	Draw the block diagram of a bidirectional shift register.	**04**
	(c)	Explain detailed effect of transistor, temperature and collector current on βdc	**07**

Q.5	**(a)**	Define Intrinsic and Extrinsic semiconductors. Draw the same using Silicon crystals atomic distribution for a trivalent and pentavalent atom each.	**03**
	(b)	Draw the ideal curve for a diode in Forward bias and Reverse bias condition.	**04**
	(c)	Explain the working of a Bridge Full Wave Rectifier circuit. Use relevant circuit diagrams and waveforms.	**07**

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Q.5	**(a)**	Evaluate the PIV for a half wave rectifier circuit, for a center tapped and a bridge full wave rectifier circuit.	**03**
	(b)	A 5V sinusoidal signal is given as input. It is desired to clip the positive half of the waveform to operate the next stage. Design the circuit for the same.	**04** **07**
	(c)	Define DC load line and Q-point of operation with the help of diagrams. How biasing plays an important role in the same? Explain fixed biasing.	

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