Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV(New) • EXAMINATION – WINTER 2016

Subject Code:2140910 Date:19/11/2016

Subject Name: Digital Electronics

Time:02:30 PM to 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Answer the following Questions: **14**

1 $(26.24)_8$ = ($)_{10}$

2 $(68BE)_{16}$ = ($)_8$

3 $(127.625)_{10}$ = ($)_2$

4 Determine the value of base b if $(263)_{10} = (107)_b$

5 Multiply $(1011)_2$ and $(101)_2$ without converting to decimal

6 Perform the subtraction $(10011)_2$-$(10001)_2$ using 2's complement method.

7 Obtain 10's complement of $(349)_{10}$

8 $(479)_{10}$ = ($)_{BCD}$

9 $(509)_{10}$ = ($)_{Excess-3}$

10 $(10111011)_2$ = ($)_{gray\ code}$

11 A code with minimum Hamming distance three is able to correct_____errors and detect_____errors

12 Define Hamming Code.

13 Why are NAND and NOR gates known as universal gates?

14 Differentiate between combinational logic circuit and sequential logic circuit.

Q.2 (a) Prove that a positive-logic AND gate is a negative-logic OR gate. **03**

(b) Write truth table for 3-bit odd parity generator and draw its logic diagram. **04**

(c) Simplify the Boolean function F = A'B'C'+AB'D+A'B'CD' using don't-care conditions d=ABC+AB'D' in (i) sum of products and (ii) product of sums by means of Karnaugh map and implement it with no more than two NOR gates. Assume that both the normal and complement inputs are available. **07**

OR

(c) Simplify the Boolean function $F(x_1,x_2,x_3,x_4)=\Sigma m(0,5,7,8,9,10,11,14,15)$ using tabulation method. **07**

Q.3 (a) Demonstrate by means of truth tables the validity of the De Morgan's theorems for three variables. **03**

(b) Explain typical characteristics of digital logic families. **04**

(c) Construct BCD adder using two 4-bit binary parallel adder and logic gates. **07**

OR

Q.3 (a) Explain full- subtractor in brief. **03**

(b) Simplify the following Boolean functions to a minimum number of literals. **04**
(i) F(x,y,z)=xy+xyz+xyz'+x'yz (ii) F(p, q, r, s) = (p'+q) (p+q+s)s'

(c) Explain 3-to-8 line decoder. Construct a 4 × 16 decoder with two 3 × 8 decoder. Use block diagram construction only. **07**

Q.4 (a) Explain 2-bit magnitude comparator. **03**

(b) Explain multiplexer with suitable example. **04**

(c) Differentiate between level triggering and edge triggering of flip-flops. Explain Master-Slave J-K flip-flop configuration. **07**

OR

Q.4 (a) Explain operation of clocked S-R Flip-Flop. **03**

	(b)	Design 2-bit synchronous binary up counter using J-K flip-flop.	**04**
	(c)	Explain BCD ripple counter with logic diagram and timing diagram.	**07**
Q.5	**(a)**	Explain concept of shift registers.	**03**
	(b)	Compare between various types of ROM.	**04**
	(c)	Explain the concept of RAM. Explain working of any one type of RAM.	**07**

OR

Q.5	**(a)**	Mention the applications of D/A converter and A/D converter.	**03**
	(b)	Describe the operation of R-2R ladder D/A converter in brief.	**04**
	(c)	Explain working of Successive-Approximation-Register A/D converter. Compare it with Flash A/D converter.	**07**

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