Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV(New) • EXAMINATION – WINTER 2016

Subject Code:2141001 **Date:19/11/2016**

Subject Name:Microprocessor and Interfacing

Time:02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	Which of the following is Non-Maskable interrupt in 8085? a) INTR b) RST 5.5 c) TRAP d) none of these	
	2	Which of the following register maintain the sequence of execution in 8085? a) PC b) Accumulator c) SP d) none of these	
	3	Which of the following is not a 3 BYTE instruction? a) LXI B,1000H b) LDA 1500H c) DAD B d) CALL 2500H	
	4	Which of the following instruction requires ONLY ONE machine cycle for execution? a) INR M b) ADC B c) MVI A,52H d) none of these	
	5	Which of the following instruction does not affect ZERO flag? a) ADD B b) DCR B c) SUI 20H d) DCX B	
	6	Stack memory in 8085 operates with which mechanism? a) FIFO b) FILO c) LIFO d) LILO	
	7	Which of the following instruction requires opcode fetch machine cycle of 6 T-states? a) PUSH PSW b) RET c) POP PSW d) MVI A,25H	
	8	How many address lines are available in 8085?	
	9	What is the value of program counter after reset in 8085?	
	10	What is the value of clock frequency in 8085, if the crystal frequency used is of 6 MHz?	
	11	How many address lines are directly connected for the memory of 4K X 8 bits?	
	12	How 8085 microprocessor can come out from HALT state?	
	13	What is the vector location for the interrupt RST 6.5?	
	14	How many data lines are available in 8086 microprocessor?	
Q.2	**(a)**	Explain the flag register and flag bits of 8085.	**03**
	(b)	Draw the timing diagram of instruction MOV C,A	**04**
	(c)	What is addressing mode? State the addressing modes of the following instructions i) MOV A,B ii) LDA 2500H iii) ANA M iv) LXI SP,FFFFH v) CMA vi) XRI 78H	**07**

OR

	(c)	Design a delay loop which can generate a delay of 5msec. Assume that the clock frequency of 8085 microprocessor is 2 MHz.	**07**
Q.3	**(a)**	Draw the circuit to generate four control signals from RD', WR' and IO/M' in 8085.	**03**
	(b)	Differentiate between absolute and partial decoding techniques.	**04**
	(c)	Write a program in 8085 assembly language to separate numbers between 15H & 50H (inclusive 15H & 50H) from the given array of five elements. Assume that the input array is available from memory location 2500H and store separated numbers from 2600H memory locations onwards.	**07**

OR

Q.3	**(a)**	Draw the circuit diagram to demultiplex AD0 – AD7 multiplexed address and data lines.	**03**
	(b)	Specify the register contents and the flag status after each of the following instructions is executed. Specify the output at PORT0.	**04**

	A	B	S	Z	CY
Initial values ➔	00h	ffh	0	1	0

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MVI A,F2H
MVI B,7AH
ADD B
OUT PORT0
HLT
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	(c)	Design 8085 microprocessor based system to interface an EROM of 4K Bytes having starting address 0000h and RAM memory of 4K Bytes having starting address 4000H.	**07**
Q.4	**(a)**	List out the priorities of hardware interrupts in 8085.	**03**
	(b)	Write a program in 8085 assembly language to exchange the contents of HL and DE register pairs without using XCHG and MOV instructions. (i.e. if the contents of DE and HL pair before execution 1234H and 5678H respectively then after the program execution the contents of DE and HL must be 5678H and 1234H respectively)	**04**
	(c)	Compare I/O mapped I/O and memory mapped I/O with respect to 8085 microprocessor.	**07**

OR

Q.4	**(a)**	Justify "software reset/restart instruction is one byte call instruction".	**03**
	(b)	Explain RIM and SIM instructions of 8085 microprocessor.	**04**
	(c)	Explain the pipeline architecture of 8086 microprocessor.	**07**
Q.5	**(a)**	Explain three control flag bits of 8086 microprocessor.	**03**
	(b)	Explain the Mode 0 and Mode 3 of 8254/8253.	**04**
	(c)	List out the features of 8255 and explain the control word format of 8255 in detail.	**07**

OR

Q.5	**(a)**	How many address lines available in 8086, 8088, 80186, 80286, 80386 & 80486 microprocessors?	**03**
	(b)	Explain the function of Interrupt Request Register (IRR) and Priority Resolver in 8259 (Priority Interrupt Controller).	**04**
	(c)	Show the schematic how 8237 DMA controller works with 8085 microprocessor. List out the steps for copying 100 bytes of data from peripheral device to memory using 8237 (highlighting activation/deactivation of all important pins for handshaking).	**07**

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