Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER–IV(New) • EXAMINATION – WINTER 2016**

**Subject Code:2142406** **Date:22/11/2016**

**Subject Name:Digital Electronics and its applications**

**Time:02:30 PM to 05:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q1 Fill in the blanks. (14)

(1) 101.10 = ( _____)H
(2) Representation of 10108 in 16 bit binary number is ( _____ )$_2$
(3) 101.102= ( _____ )$_8$
(4) 1001 = ( _____ )BCD
(5) 1 Byte = ( _____ ) Bits
(6) Multiplexure is _____ circuit. (Sequential, Combinational, Counter, Analog)
(7) _____ can not be used to implement combinational circuit. (NAND Gate, NOR Gate, MUX, Decoder, Latch)
(8) 7400 is an IC built with _____ logic. (CMOS, ECL, TTL, DTL)
(9) Gray code after 1000 is _____.
(10) 12BCD + 67BCD = ( _____ )16
(11) $1010 \times 1010_2$ = _____
(12) ABC can be represented alternatively by _____.
(13) Sequential circuit must include _____ for operation.
(14) Fastest logic family is _____.

Q2 (a) Compute 101X $101_2$ (3)

(b) Represent - 1in 16 bit ’2s complement form. (4)

(c) represent NOT,and two input NAND, AND, OR, NOR, XOR, XNOR Gates using NOR gate. Also draw schemetic for these representations. (7)

OR

(c) Simplify function F(a,b,c,d) = ∑ m(0,1,2,4,5,6,8,9,12,13,14) using K Map. (7)

Q3 (a) What is universal gate? State gates which are used as universal gates. (3)

(b) Suppose A and B are two input bits and Cin is carry input. S and Co are sum and output carry respectively. Prepare truth table for half adder and full adderfor these signals. Also, write logical equations for S and Co. (4)

(c) Obtain the truth table of F)x, y, z (= (x’ +y) (y’ + z) and express F in SOP and POS form. (7)

OR

Q3 (a) What is decoder? State applications of decoder. (3)

(b) Design full adder circuit using decoder. (4)

(c) Reduce function F(a,b,c,d) = Π M(4,6,11,14, (15and prepare schematic for the reduced function using MUX. (7)

Q4 (a) Define sequential circuit and draw its block diagram. (3)

(b) Define Latch and Flip Flop. (4)

(c) Design a 3 bit gray code counter with ‘000’ as initial count value. (7)

OR

| | | | |
|---|---|---|---|
| Q4 | (a) | Draw internal schematic of JK flip flop.<br>Also give truth table of JK flip flop. | (3) |
| | (b) | Explain how JK flip flop can be used to implement D flip flop. | (4) |
| | (c) | Design a 3bit couter which will count sequence 000,001,011, 100only once. | (7) |
| Q5 | (a) | Draw schematic diagram of master slave flip flop. | (3) |
| | (b) | Define state and state diagram. | (4) |
| | (c) | With reference to register data transfer implement the hardware for statement x'T :1A←B (Assume x is input, T 1is timing input, A & B are the registers). | (7) |

OR

| | | | |
|---|---|---|---|
| Q5 | (a) | State various types of memory. | (3) |
| | (b) | Define (1) Accumulator (2) ALU register | (4) |
| | (c) | Explain shift register and state its applications. | (7) |

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