

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-V(New) • EXAMINATION – WINTER 2016****Subject Code:2151007****Date:30/11/2016****Subject Name:Digital Design****Time:10:30 AM to 01:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 Do as Directed [14]**
- 1 Explain variable in VHDL.
 - 2 State importance of configuration.
 - 3 Explain positional association and named association in the port map clause.
 - 4 Write entity declaration for half adder.
 - 5 Explain 'Wait statement'.
 - 6 List the 9 values of std_logic.
 - 7 Declare 4-element array of 8-bit std_logic_vector called array_8.
 - 8 What is difference between STD_LOGIC and STD_ULOGIC?
 - 9 Declare an enumerated data type called VOWEL containing only vowel characters.
 - 10 Is this statement $x <= y$ after 5 ns synthesized or not?
 - 11 Every signal in a sensitivity list of a statement must change to fire the statement. True or False?
 - 12 The order of execution of concurrent VHDL statements cannot be predicted. True or False?
 - 13 One entity may be assigned to many architecture bodies. True or False?
 - 14 Mealy machine requires more state than moore machine to do same job. True or False?
- Q.2 (a) Differentiate between a process and wait statement. Can they be used simultaneously in a program? [03]**
- (b) List the major capabilities of VHDL along with the features. [04]**
- (c) Explain data types used in VHDL. [07]**
- OR**
- (c) Explain various predefined operators in VHDL with their precedence. [07]**
- Q.3 (a) Explain BLOCK statement. [03]**
- (b) Differentiate between concurrent and sequential signal assignment statement. [04]**
- (c) Discuss types of FSM (finite state machine) with appropriate example. [07]**
- OR**
- Q.3 (a) How will you compare component declaration and component instantiation? [03]**
- (b) What is the use of assertion statement? Explain with example. [04]**
- (c) Discuss various loops in VHDL and explain 'Generate' statement in VHDL with an example. [07]**
- Q.4 (a) Differentiate between exit and next statements. [03]**
- (b) Give difference between signal and variable [04]**
- (c) Write code for 4x1 MUX with structural modeling. [07]**

OR

- Q.4** (a) What is delta-delay? What is its effect in VHDL? [03]
(b) Write VHDL code for 2x4 decoder with structural modelling. [04]
(c) Write VHDL code to implement 4-bit ring counter using behavioral modeling. [07]
- Q.5** (a) What is test bench? Write typical test bench format. [03]
(b) Write VHDL code to implement positive edge triggered D flip-flop [04]
(c) What is FPGA? Draw its basic structure and give its applications. [07]

OR

- Q.5** (a) Explain PLA with necessary diagrams. [03]
(b) Write VHDL code of clock divider to get 1 Hz clock from 1 MHz clock input. [04]
(c) Explain Programmable Logic devices. Also give comparison between PAL, PLA, CPLD and FPGA [07]
