Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER – VI (NEW).EXAMINATION – WINTER 2016

Subject Code: 2160709 **Date: 26/10/2016**

Subject Name: Embedded & VLSI Design

Time: 02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain different classification of Embedded Systems? Give an example of each.	**07**
	(b)	Explain the concept of Static Memory (SRAM) Cell. Explain the merits and limitation of SRAM and DRAM as Random Access Memory.	**07**
Q.2	**(a)**	What is EDLC? Explain different phases of Embedded Product Development Life Cycle.	**07**
	(b)	Explain the fabrication steps of nMOS transistor with necessary figures.	**07**
		OR	
	(b)	Explain VLSI Design flow using Y-chart.	**07**
Q.3	**(a)**	What is the need of Scaling? Discuss constant voltage scaling in detail with its merits and demerits.	**07**
	(b)	Calculate noise margin and V_{th} of the circuit for CMOS inverter with following parameters: VDD = 3.3 V, For NMOS $V_{TO,n}$ = 0.6 V, μ_n Cox=60 μ A/V^2 , (W/L)n=8 For PMOS $V_{TO,p}$ = - 0.7 V, μ_p Cox=25 μ A/V^2 , (W/L)p=12.	**07**
		OR	
Q.3	**(a)**	Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points V_{OH}, V_{OL} , V_{IH} and V_{IL} for depletion- load nMOS inverter.	**07**
	(b)	Consider a MOS system with the following parameters: t_{ox} =200Å ,Φ_{GC} = - 0.85 V, *NA*= 2*1015 cm^{-3},*Qox*= *q** 2 *10^{11} C/cm^2 Determine the threshold voltage V under zero bias at room temperature (T = 300° K). Note that ε_{ox}=3.97ev and ε_{si}=11.7eV.	**07**
Q.4	**(a)**	Define τ_{PHL} and τ_{PHL} .Derive expression for propagation delay times τ_{PHL} and τ_{PHL} for CMOS Inverter.	**07**
	(b)	Explain NAND gate using CMOS realization, pass transistor and Complementary pass transistor realization.	**07**
		OR	
Q.4	**(a)**	Discuss CMOS transmission gate for all operating regions and plot equivalent Resistance of CMOS transmission gate as a function of output voltage.	**07**
	(b)	Explain switching power dissipation of CMOS inverter.	**07**
Q.5	**(a)**	Draw CMOS negative edge-triggered master-slave D flip-flop and explain its	**07**

working.

	(b)	Explain BIST techniques.	**07**

OR

Q.5	**(a)**	What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis.	**07**
	(b)	Explain Latch up problem in CMOS inverter. Mention causes and remedy for avoiding latch up	**07**

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