Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER – VI (NEW).EXAMINATION – WINTER 2016

Subject Code: 2161004 **Date: 26/10/2016**

Subject Name: VLSI Design

Time: 02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain the importance of Regular, Modular and Local Architecture for VLSI. Also give one example for each. **07**

(b) Explain the fabrication steps of NMOS transistor with necessary figures **07**

Q.2 **(a)** What do you understand by gradual channel approximation? Derive expression for the drain current flowing through n-channel MOSFET as a function of V_{GS}, V_{DS}, and V_{BS}. **07**

(b) Calculate the threshold voltage V_{TO} at V_{SB}= 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: **07**

Substrate doping density $N_A=10^{16}cm^{-3}$,
Polysilicon gate density $N_D=2 \times 10^{20}cm^{-3}$,
Gate oxide thickness t_{ox}=500 Angstrom and
Oxide interface fixed charge density $N_{ox}= 4 \times 10^{10}cm^{-2}$,
φ_F(gate) = 0.55V.

Physical constants :
Thermal voltage =KT/q = 0.026 volt.
Energy Gap of silicon (Si) =E_g = 1.12 Ev.
Intrinsic Carrier Concentration of silicon=$n_i=1.45x10^{10}cm^{-3}$.
Dielectric constant of vaccume =ε_o=8.85 x 10-^{14}F/cm.
Dielectric constant of silicon =ε_{si}= 11.7 x ε_oF/cm.
Dielectric constant of silicon dioxide =ε_{ox}= 3.97 x ε_o F/cm

OR

(b) For an enhancement type NMOS transistor V_{T0}= 0.8 V , λ= 0.05 1/V , process transconduction μ_n *C_{ox}=20A/V^2, W/L =20μm , γ=0.2 $V^{1/2}$,2∅F=0.58 VV$_G$= 5V , V_D=4V, V_S=2V. Calculate Drain Current I_D **07**

Q.3 **(a)** Draw the inverter circuit with depletion type NMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points V_{OH}, V_{OL} and V_{IL} and V_{IH} for depletion- load NMOS inverter **07**

(b) Explain Elmore delay model for CMOS inverter with appropriate diagram and explain how rise time and fall time are computed if inverter is driving another inverter **07**

OR

Q.3 **(a)** Define τ_{PHL} and τ_{PLH} for CMOS inverter. Draw input and output waveforms during high to low transition of output for a CMOS inverter Derive τ_{PHL} for CMOS inverter **07**

(b) Design a resistive load inverter with R = 1kΩ, such that VOL = 0.6V. The enhancement-type nMOS driver transistor has the following parameters: **07**

V_{DD} = 5.0V,V_{TO} = 1.0 V, γ = 0.2 $V^{1/2}$,λ = 0,μ_n*Cox = 22.0 μA/V^2

a. Determine the required aspect ratio, W/L.

b. Determine V_{IL} and V_{IH}.

Q.4 **(a)** What is Euler path approach? Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), X =A(D + E) + BC . Explain the importance of Euler path approach. **07**

(b) Draw negative edge triggered Master slave D flip flop and explain its working **07**

OR

Q.4 **(a)** Explain the basic principle of pass transistor, using Logic "1" transfer event and logic "0" event. For the NMOS pass transistor circuit shown in figure 1 below, find Vo. **07**

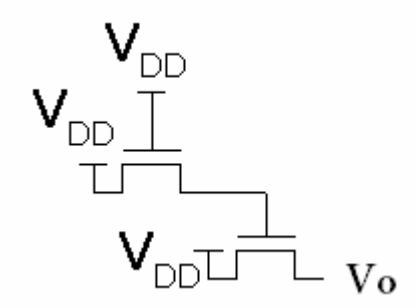

Figure 1

(b) Write a short note on CMOS Transmission Gate. Explain its usefulness. Draw 2:1 MUX using compound gate and compare it with 4:1 MUX based on transmission gate. Also draw 8:1 MUX based on transmission gate **07**

Q.5 **(a)** What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis. **07**

(b) List Ad-hoc testable design techniques and discuss any two in detail **07**

OR

Q.5 **(a)** Write a short note on Built In Self Test (BIST). **07**

(b) Why do we need isolation between MOS transistors fabricated on a single chip? Explain etched field-oxide isolation and LOCOS isolation techniques with diagrams **07**

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