Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER – VI (NEW).EXAMINATION – WINTER 2016

Subject Code: 2161101 **Date: 26/10/2016**

Subject Name: VLSI Technology & Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **14**

Define following Terms:

1 Etching
2 Threshold Voltage
3 Noise Margin
4 Metallization
5 Body Effect
6 Propagation Delay
7 Stuck at Fault

Short Questions:

1 What is the application of PLA?
2 Which material is used for gate oxide in MOS technology?
3 What is the fundamental difference between MOSFET and BJT?
4 What happens to delay if you increase load capacitance?
5 Which MOSFET is used in pass transistor logic?
6 Write Full Form of SPLD
7 What are three main domains in Y chart of VLSI Design flow?

Q.2 **(a)** What are the advantages of ion implantation over diffusion? **03**

(b) Why nMOS is better then pMOS transistor? **04**

(c) Explain the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region. **07**

OR

(c) Write down the steps with neat sketch for fabrication of PMOS. **07**

Q.3 **(a)** Write I-V equation of P channel MOSFET for all Regions. **03**

(b) Calculate the drain current of nMOS if source terminal is connected to ground and **04**

Vg = 1.8V Vd = 1 V Vth = 1V

μn= 400 cm^2/VS Cox = 800uF (W/L)n=1.5

(c) For a CMOS inverter with following specification compute V_{IL} , V_{IH} and find out inverter is symmetric or not? **07**

V_{DD} = 1.8V Vtn= 0.5 V Vtp= -0.5 V

μn= 580 cm^2/VS μp= 290 cm^2/VS

(W/L)p = 2(W/L)n

OR

Q.3	**(a)**	Describe different types of photo resist materials.	**03**
	(b)	Explain Channel length modulation.	**04**
	(c)	Give the comparison of resistive load ,depletion load and CMOS inverter circuits.	**07**
Q.4	**(a)**	Explain the concept of MOSFET as a switch.	**03**
	(b)	Compare Static and Dynamic CMOS logic circuits.	**04**
	(c)	Derive the equation of propagation delay.Describe the different ways to minimize Propagation Delay?	**07**
		OR	
Q.4	**(a)**	Explain FPGA and CPLD	**03**
	(b)	Explain Voltage bootstrapping.	**04**
	(c)	Implement the function using Depletion load Inverter And CMOS : f = AB + C	**07**
Q.5	**(a)**	Implement CMOS SR latch based on NAND gates.	**03**
	(b)	What is static and dynamic power dissipation?	**04**
	(c)	Discuss RACE problem in Dynamic logic structure.	**07**
		OR	
Q.5	**(a)**	What do you understand by clock skew?	**03**
	(b)	Explain Transmission Gate with example.	**04**
	(c)	What is Latch up? Explain the prevention techniques.	**07**

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