## **GUJARAT TECHNOLOGICAL UNIVERSITY** B. E. - SEMESTER – III • EXAMINATION – WINTER 2012

Su	bject	code: 130902 Date: 04-01-2013	
Su	bject	Name: Analog and Digital Electronics	
Tiı	ne: 1	0.30 am – 01.00 pm Total Marks: 70	
Ins	struc	tions:	
	1.	Attempt all questions.	
	2. 3.	Make suitable assumptions wherever necessary. Figures to the right indicate full marks.	
Q.1	(a)	Draw the equivalent circuit with significance of each component of a practical OP-AMP.	07
	<b>(b)</b>	List and Discuss all ideal characteristics of an Op Amp.	07
Q.2	(a)	Explain voltage follower and inverter using Op- Amp.	07
	(b)	Draw functional block diagram of IC 555 & discuss function of each pin. OR	07
	<b>(b)</b>	Explain integrator with its frequency response.	07
Q.3	(a)	Explain the Universal Gate and build up AND, OR and NOT using NAND and NOR gate.	07
	<b>(b</b> )	Derive Full Adder with the help of necessary truth table, K- Map. Also express in AOI logic diagram.	07
		OR	
Q.3	<b>(a)</b>	Derive Full Subtractor with the help of necessary truth table, K- Map. Also	07
		express in AOI logic diagram.	
	<b>(b)</b>	Do as directed	07
		1) $(3F8)16 + (5B3)_{16} = ($ )16	
		2) $(231.23)4 = ()10$	
		3) $(111101100)2 = ()$ 8	
Q.4	<b>(a)</b>	Define the following general characteristics of logic families.	07
		(i) Poly (ii) Poly (ii) Power Dissination	
	(b)	1) Subtract with unsigned binary no using 2's complement of subtrahend	07
	()	:x=1010100, y=1000011, perform x-y	
		2) Subtract with unsigned binary no using 10's complement of subtrahend	
		x=3250, y=72532, perform x-y.	
		OR	
Q.4	(a)	Simplify the following	07
		1) $xy + xyz + xyz' + x'yz$	
0.4	<b>(1</b> -)	2) $x + x'y + xy'$ Cive electric of maximum Discuss 4 with huffer maximum D flin flor	07
Q.4	(D) (D)	Give classification of registers. Discuss $4 - bit buffer register using D - flip flopi) Minimize the following Boolean supression using K map V = \sum_{i=1}^{n} V_{i}$	07
Q.5	(a)	(0,1,4,8,9,10) $Y = 2m$	07
		11) Discuss multiplexers with suitable diagram	~ <del>~</del>
	(b)	Explain the working of Master-Slave J-K flip-flop	07
05	(a)	UK Define decoders encoder and de multiplever Give application of each	07
Q.5	(a) (h)	State and explain the triggering methods for a T <sub>-</sub> flip flop	07
	(U)	suite and explain the differing memory for a 1- mp mp.	07

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