Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

B. E. - SEMESTER – VI • EXAMINATION – WINTER 2012

Subject code: 161004 Date: 05/01/2013

Subject Name: VLSI Technology and Design

Time: 02.30 pm - 05.00 pm Total Marks: 70

Instructions:

1. **Attempt any five questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Discuss following approaches (with examples) used to reduce complexity of IC design: 1. Hierarchy, 2. Regularity, 3. Modularity, and 4. Locality. **07**

(b) Why do we need isolation between MOS transistors fabricated on a single chip? Explain etched field-oxide isolation and LOCOS isolation techniques with diagrams. **07**

Q.2 **(a)** Draw layout of CMOS Inverter and indicate minimum eight layout rules of your choice in terms of λ. **07**

(b) Derive expression for the maximum possible depth of the depletion region in two-terminal MOS structure. **07**

OR

(b) Calculate the threshold voltage for a polysilicon gate nMOS transistor with the following parameters: $N_A = 2 \times 10^{16}$ cm^{-3}, $N_D = 2 \times 10^{19}$ cm^{-3}, $t_{ox} = 300 \times 10^{-8}$ cm, and $N_{ox} = 10^{10}$ cm^{-2}. Take kT/q = 26 mV, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $q = 1.6 \times 10^{-19}$ C, $\varepsilon_{ox} = 3.97 \times 8.85 \times 10^{-14}$ F/cm, $\varepsilon_{si} = 11.7 \times 8.85 \times 10^{-14}$ F/cm. **07**

Q.3 **(a)** What do you understand by gradual channel approximation? Derive expression for the drain current flowing through n-channel MOSFET as a function of V_{GS}, V_{DS}, and V_{BS}. **07**

(b) Derive expressions for V_{IH} and V_{IL} for CMOS Inverter. **07**

OR

Q.3 **(a)** Explain constant field scaling device reduction strategy and show that the power density does not change in a device scaled using this technique. **07**

(b) Discuss the effect of supply voltage scaling on VTC (voltage transfer characteristic) of CMOS Inverter. What is the minimum V_{DD} below which VTC exhibits hysteresis effect? **07**

Q.4 **(a)** Define propagation delay and derive expression for τ_{PHL} for CMOS Inverter. Assume ideal step as an input to CMOS Inverter. **07**

(b) Draw two-input CMOS NOR gate and obtain expression for switching threshold voltage (v_{th}). Assume that both NMOS transistors are identical. Similarly, PMOS transistors are also identical. **07**

OR

Q.4 **(a)** Obtain expression for switching power dissipation in CMOS Inverter circuit. Assume ideal step as an input to CMOS Inverter. Under what constraints, derived expression can be applied to any CMOS logic circuit? **07**

	(b)	Justify importance of transmission gate. Draw six-transistor CMOS transmission gate implementation of the XOR function. Verify its functionality.	**07**
Q.5	**(a)**	Draw CMOS negative edge-triggered master-slave D flip-flop and explain its working.	**07**
	(b)	Explain cascading problem observed in dynamic CMOS logic. What are the different approaches to solve this problem?	**07**

OR

Q.5	**(a)**	What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis.	**07**
	(b)	List out possible electrical and logical faults observed in the circuit. Define controllability and observability.	**07**

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