Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV • EXAMINATION – WINTER 2013

Subject Code: 140701 Date: 19-12-2013

Subject Name: Microprocessor and Interfacing

Time: 02:30 pm to 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following. **07**

(1) What are the advantages of Assembly language in comperision with High level languages?

(2) What are Tri-state devices and why are they essential in a Bus oriented system?

(b) Some of the pins of 8085 are listed below .For each pin show whether it is an input line or an output line and mention its function. **07**

(1) ALE (2) SOD (3) IO/ $\overline{M}$

(4) READY (5) HOLD (6) $\overline{RD}$

Q.2 **(a)** Distinguish between the following pairs of instructions. (Any Two) **07**

(1) LXIH 1234H and LHLD 1234H

(2) RAL and RLC

(3) JMP 1000H and CALL 1000H

(b) Make comparision between Memory mapped I/O and I/O Mapped I/O. **07**

OR

(b) What do you understand by the term Addressing Modes? Explain, giving suitable , all the addressing modes supported by 8085. **07**

Q.3 Write ALP, along with flow chart, for the following. **14**

(a) Two ASCII strings start at memory locations 1042H and 1052H respectively. Memory location 1041H contains the length of the strings. The program sets the memory location 1040H to 00H, if the strings are equal and to FFH if they are not.

(b) A binary number is stored in memory location 3040H convert it to BCD number and store BCD1 (least significant BCD digit) into memory location 3041H and BCD2 and BCD3 in memory locations 3042H and 3043H respectively.

OR

14

Q.3 Write ALP, along with flow chart, for the following.

(a) A data array of length 16 (Decimal) has been stored in ascending order starting from memory location 3000H to 300FH. Write an ALP to store the data in decending order from memory location 3000H to 300FH (ie. In the same original space)

(b) Write a ALP to count from 00 to 20H with a delay of 100 ms. between each count. After the count 20H, the counter should reset itself and repeat the sequence. Use register pair DE as a delay register. Draw a flowchart and show your approximate delay calculations for 100ms.delay. The clock freq. is 1Mhz. Assume suitable value of T states for the delay calculation.

Q.4 **(a)** Explain Linear select decoding. Compare it with Absolute decoding. **07**

(b) Explain the block diagram of 8259 Programmable interrupt controller. What are its features? Explain the interrupt operation of 8259 in the simplest format. **07**

OR

Q.4 **(a)** STA instruction requires 5 machine cycles and 13T states. Explain using timing diagram sequence of events taking place in each machine cycle with reference to 3000H ……STA 4000H instruction. **07**

(b) Sketch and explain scheme of interfacing one input and one output device using gates and a 3 to 8 decoder with two $\overline{EN}$ and one EN input. Both devices should have the address FAH. **07**

Q.5 **(a)** Explain RIM and SIM instructions. **07**

(b) With the help of block diagram explain the internal architecture of IC 8255 and describe its working in BSR mode. **07**

OR

Q.5 **(a)** Draw and explain the block diagram of 8251 USART. **07**

(b) Write short note on any one of the following. **07**

(1) 8237 DMA controller.

(2) 8279 Keyboard / Display interface.

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