Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI • EXAMINATION – WINTER 2013

Subject Code: 161004 Date: 06-12-2013

Subject Name: VLSI Technology and Design

Time: 02:30 pm to 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** What is the difference between positive photoresist and negative photoresist? Which is commonly used in the manufacturing of high density integrated circuits? **03**

(b) Why do we require device isolation between MOS transistors that comprise an IC? Explain LOCOS isolation technique with necessary diagrams. **04**

(c) Discuss following criteria which are considered to measure the quality of chip design. 1. Testability 2. Yield and manufacturability 3. Reliability 4. Technology updateability **07**

Q.2 **(a)** Draw circuit of resistive load inverter. Derive V_{IL},V_{IH} and V_{OL} for resistive load inverter. **07**

(b) Calculate the threshold voltage V_{TO} under zero bias at room temperature (T=300ºK), for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 10^{20}$ cm^{-3}, t_{ox} = 500ºA, and oxide interface fixed charge density $N_{OX} = 2 \times 10^{10}$ cm^{-3}. Take $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, $\varepsilon_{si} = 11.7 \times \varepsilon_0$ F/cm, $\varepsilon_{ox} = 3.97 \times \varepsilon_0$ F/cm. **07**

OR

(b) Consider the CMOS inverter, with the following device parameters: **07**

nMOS $V_{TO,n} = 0.6$ V $\mu_n C_{ox} = 60\ \mu A/V^2$

pMOS $V_{TO,p} = -0.8$ V $\mu_p C_{ox} = 20\ \mu A/V^2$

Also: $V_{DD} = 3V$, $\lambda = 0$.

a. Determine the (W/L) ratios of the nMOS and the pMOS transistor such that the switching threshold is $V_{th} = 1.5V$.

b. Calculate noise margin.

Q.3 **(a)** Explain the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region. **07**

(b) For a CMOS inverter circuit, derive its critical voltage points V_{IL} and V_{IH}. **07**

OR

Q.3 **(a)** What is short channel effect? Derive expression for the change in threshold voltage due to short channel effect. **07**

(b) What is constant voltage scaling? How delay time, power density and power dissipation are affected in a device scaled with constant voltage scaling. **07**

Q.4 **(a)** Explain Elmore delay calculation method for complex RC network. Derive the formula for Elmore delay τ_{DN}. **07**

(b) Explain two input depletion load NOR gate and derive the necessary equations for the same. **07**

OR

Q.4 **(a)** For XOR function, draw following implementations. **07**

1. Full CMOS gate
2. Pseudo-nMOS gate
3. CMOS transmission gate(TG)

(b) Explain the principle of dynamic CMOS logic (Precharge-Evaluate logic). Discuss its advantages and disadvantage. **07**

Q.5 **(a)** Draw CMOS implementation of D latch with two inverters and two CMOS TG gates. Explain its working. **07**

(b) What is the need of voltage bootstrapping? Draw dynamic boot-strapping arrangement and explain it. **07**

OR

Q.5 **(a)** Discuss remedies of CMOS Latch-Up. **07**

(b) Ad hoc testable design techniques. **07**

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