Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – WINTER • 2014

Subject Code: 130701 **Date: 23-12-2014**

Subject Name: Digital Logic Design

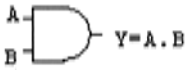
Time: 02.30 pm - 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following questions **07**

1. Find out Y, if B=1 and A=square wave



2. Add the two numbers $(A3E5)_{16}$ + $(CDA4)_{16}$
3. explain SSI, MSI, LSI and VLSI

(b) 1. Do subtraction using 12 bit two's complement method **07**
27.125 – 79.625
2. Do BCD addition for given numbers
679.6 + 536.8

Q.2 **(a)** Reduce using K-map **07**
Σ m (0, 2, 6, 10, 11, 12, 13) + d (4, 5, 14, 15)

(b) Obtain the set of prime implicants for Σ m (0, 1, 6, 7, 8, 9, 13, 14, 15) **07**

OR

(b) Obtain the set of prime implicants for Π M (2, 3, 8, 12, 13) . d (10, 14) **07**

Q.3 **(a)** Design a combinational circuit that multiplies BCD inputs by 5. Show that output can be obtained from the inputs without using any logic gates. **07**

(b) Design a combinational circuit that accepts the Decimal number in BCD and display it on Seven segment display. **07**

OR

Q.3 **(a)** Implement F (A, B, C, D) = Σ m (0, 1, 3, 4, 8, 9, 15) using multiplexer, choose A as input line. **07**

(b) Design a synchronous BCD counter with JK Flip flop. **07**

Q.4 **(a)** 1. Convert J K Flip Flop to S R Flip flop. **07**
2. Show the logical diagram of clocked S R Flip flop with AND and NOR gates.

(b) Draw and explain Master- Slave Flip flop. **07**

OR

Q.4 **(a)** Design and explain 4-bit Ripple UP/DOWN Counter using positive edge triggered Flip flop. **07**

(b) Design and implement a Modulo-6 Asynchronous counter using T Flip flop. **07**

Q.5 **(a)** Explain the design of Arithmetic Logic Design. **07**

(b) Explain the digital IC Parameters. **07**

1. Fan in, Fan out
2. Propogation Delay
3. Power Dissipation
4. Noise Margin

OR

Q.5 **(a)** 1. Give comparison for TTL and CMOS family. **07**
2. Implement basic gates using DTL logic.

(b) Explain Register Transfer Micro Operation and Arithmetic Micro Operations **07**

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