## **GUJARAT TECHNOLOGICAL UNIVERSITY** BE - SEMESTER-IV • EXAMINATION – WINTER • 2014

BE - SEIVIESTER-IV • EAAIVIINATION – WINTER • 2014			
Subject Code: 141101Date: 29-12-2014Subject Name: Advance ElectronicsTotal Marks: 70Time: 02:30 pm - 05:00 pmTotal Marks: 70			
Instructions: 1. Attempt all questions. 2. Make suitable assumptions wherever necessary. 3. Figures to the right indicate full marks.			
Q.1	(a) (b)	Draw hybrid $\pi$ equivalent circuit for common emitter transistor. Also derive the expression for input conductance $(g_{b'e})$ . Write a short note on two stages RC – Coupled amplifier.	07 07
Q.2	(a)	Define the following terms: (1) Rise time (3) Non linear distortion (5) CMRR (7) Tilt (2) Noise margin (4) Slew rate (6) Fan out	07
	<b>(b</b> )	Draw the basic block diagram of op-amp and explain each block. OR	07
	<b>(b</b> )	What is an op-amp? List out the characteristics of ideal op-amp. Derive the expression of voltage gain for closed loop inverting amplifier.	07
Q.3	(a) (b)	Draw and explain current series feedback amplifier. Define positive and negative feedback. Also derive the expression of transfer gain with positive and negative feedback with the use of block diagram. <b>OR</b>	07 07
Q.3	(a) (b)	Derive output resistance for voltage shunt feedback amplifier and current shunt feedback amplifier. List out the steps to identify feedback topology and analysis of a feedback	07 07
	(0)	amplifier.	07
Q.4	(a)	Classify the oscillator. Also explain RC-phase shift oscillator with neat circuit diagram.	07
	(b)	In a transistorized Hartley oscillator the two inductances are 2mH and $20\mu$ H while the frequency is to be changed from 950kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied. OR	07
Q.4	( <b>a</b> )	What is an oscillator? State and derive the Barkhausen criterion required for oscillation.	07
	<b>(b</b> )	What is differential amplifier? Draw and explain emitter coupled differential amplifier.	07
Q.5	(a) (b)	Give the comparison between various logic families. Write short note on: 3-bit R-2R ladder type DAC.	07 07
Q.5	(a) (b)	<b>OR</b> Classify the logic families. Draw and explain 2-input DTL NAND gate. Draw and explain the counter type A/D converter.	07 07

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