Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI • EXAMINATION – WINTER • 2014

Subject Code: 161004 Date: 05-12-2014

Subject Name: VLSI Technology and Design

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Which are the four general criteria to measure design quality of a fabricated integrated circuit (chip)? Briefly explain each of them. **07**

(b) What are the problems associated with LOCOS isolation technique? Explain each of the fabrication steps involved in LOCOS technique with suitable diagrams. **07**

Q.2 **(a)** Draw the structure of MOS capacitor and derive the expression for the maximum depth of the depletion region for the same. **07**

(b) Define threshold voltage (V_T) of MOSFET device. Which are the four physical components on which V_T depends? Derive expression for V_T. **07**

OR

(b) How can we measure following parameters of n-channel MOSFET device? Explain with necessary test set-ups. **07**

1. K_n
2. V_{T0}
3. Substrate bias coefficient (γ)
4. CLM parameter (λ)

Q.3 **(a)** Draw CMOS Inverter circuit. Obtain expressions for V_{IL} and V_{th}. **07**

(b) Describe Elmore Delay technique to estimate the delay of interconnects. **07**

OR

Q.3 **(a)** In CMOS inverter circuit, if the supply voltage is reduced below the summation of $V_{T,n}$ *and* $|V_{T,p}|$, how the output voltage will follow the change in input voltage (i.e. draw VTC and explain its behavior)? Assume that enhancement MOSFET devices are used in the CMOS Inverter circuit. **07**

(b) Derive expression for frequency of oscillation for three stage ring oscillator circuit. Draw necessary circuit and waveforms. **07**

Q.4 **(a)** Draw two-input CMOS NOR and NAND gate circuits. Identify the transistor/s suffering from body bias effect in each of these circuits. Assume single-well CMOS technology. **07**

(b) With appropriate circuit example, illustrate the cascading problem in dynamic CMOS logic and the possible solution/s for the same. **07**

OR

Q.4 **(a)** Show that the transmission gate (TG) is a good conductor of '1' as well as '0'. Implement two-input multiplexor circuit using is TGs. **07**

(b) Realize negative edge-triggered master-slave D flip-flop using CMOS transmission gates and CMOS inverters. Explain its working with waveforms. **07**

Q.5	**(a)**	Define controllability and observability. Draw and explain the general structure of scan-based design technique to improve testability of sequential circuits.	**07**
	(b)	What is the need of voltage bootstrapping? Draw MOSFET based voltage bootstrapping circuit. Explain its operation along with necessary mathematical steps.	**07**

OR

Q.5	**(a)**	What do you understand by clock skew? Explain various clock distribution schemes with diagrams.	**07**
	(b)	Draw and explain general architecture of CPLD.	**07**

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