Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII • EXAMINATION – WINTER • 2014

Subject Code: 180802 **Date: 29-11-2014**

Subject Name: VLSI Technologies

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q-1	**(a)**	Discuss VLSI design flow in brief. (Y – chart)	**7**
	(b)	Explain design procedure steps for fabrications of n-MOS transistor.	**7**
Q-2	**(a)**	Explain Channel Length Modulation.	**7**
	(b)	Explain energy band diagram of MOS structure at surface inversion and derive the equation of threshold voltage.	**7**
		OR	
Q-2	**(b)**	Explain major types of capacitances and show its variation under different operating regions and physical parameters.	**7**
Q-3	**(a)**	Draw the CMOS Inverter circuit and VTC for different operation regions of the nMOS and pMOS transistor. Derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**7**
	(b)	Discuss basic steps of the LOCOS Process.	**7**
		OR	
Q-3	**(a)**	Derive the expression for drain current as a function of V_{GS}, V_{DS} and V_{SB} for all three region of operation of MOSFET using Gradual Channel Approximation.	**7**
	(b)	Explain two different down scaling techniques for MOSFET. Which technique is preferable?	**7**
Q-4	**(a)**	Explain the functioning of depletion load nMOS inverter and derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**7**
	(b)	Concept of regularity, modularity and locality.	**7**
		OR	
Q-4	**(a)**	Explain delay time definitions for MOS Inverters Switching Characteristics and derive the Expression for λ_{PHL} & λ_{PLH}	**7**
	(b)	Writes a short note on Design Quality.	**7**
Q-5	**(a)**	Discuss Complementary pass transistor logic. Realize the XOR gate using CPL	**7**
	(b)	Explain the criteria to measure the design quality to improve the chip design and explain any two in brief	**7**
		OR	
Q-5	**(a)**	List the important concern for the IC packaging technology. Also Explain different packaging technologies.	**7**
	(b)	Write a short note on Built In Self Test (BIST).	**7**

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