Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – WINTER • 2014

Subject Code: 2131004 **Date: 20-12-2014**

Subject Name: Digital Electronics

Time: 02.30 pm - 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Select the most appropriate option. **07**

(i)Convert the decimal number 187 to 8-bit binary. 01

(A) 10111011_2 (B)11011101_2 (C) 10111101_2 (D) 10111100_2

(ii) Convert the binary number 1001.0010_2 to decimal. 01

(A) 90.125 (B) 9.125 (C) 125 (D) 12.5

(iii) If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output? 01

(A) 1 (B) 2 (C) 7 (D) 8

(iv) If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n): 01

(A) AND (B) NAND (C) NOR (D) OR

(v) When used with an IC, what does the term "QUAD" indicate?

(A) 2 circuits (B) 4 circuits (C) 6 circuits (D) 8 circuits 01

(vi) The 2's complement of the number 1101110 is
(A) 0010001. (B) 0010001. (C) 0010010. (D) None.

(vii) Which TTL logic gate is used for wired ANDing
(A) Open collector output (B) Totem Pole (C) Tri state output (D) ECL gates 01

01

(b) Minimize the following logic function using K-maps and realize using NAND and NOR gates. **07**
F(A,B,C,D) =∑_m(1,3,5,8,9,11,15) + d(2,13).

Q:2 **(a)** Minimise the logic function F (A,B,C,D) = Π_ M (1, 2, 3, 8, 9, 10, 11,14) · d (7, 15) **07**
Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only.

(b) Design a mod-12 Synchronous up counter using D-flipflop. **07**

OR

(b) Design a BCD to excess 3 code converter using minimum number of NAND gates. **07**

Q:3 **(a)** A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations **07**

A is False, B is True
A is False, C is True
A, B, C are False
A, B, C are True
(i) Write the Truth table for F. Use the convention True=1 and False = 0.
(ii) Write the simplified expression for F in SOP form.
(iii) Write the simplified expression for F in POS form.
(iv) Draw logic circuit using minimum number of 2-input NAND gates.

(b) Simplify using Boolean laws and draw the logic diagram for the given expression. **07**

$$F = \overline{ABC} + \overline{AB}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{BC} + A\,\overline{B}\,C$$

OR

Q:3 **(a)** Prove the following Boolean identities. **07**

(i) $XY + YZ + \overline{Y}\,Z = XY + Z$

(ii) $A.B + \overline{A}.B + \overline{A}.\overline{B} = \overline{A} + B$

(b) Design a 8 to 1 multiplexer by using the four variable function given by **07**

$F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$.

OR

Q:4 **(a)** Draw the circuit diagrams and Truth table of all the Flip flops (SR, D, T and JK). **07**

(b) Implement D flip flop using JK flip flop. **07**

OR

Q:4 **(a)** Define the followings. **07**

(i) Propagation delay (ii) Fan in (iii) Noise Margin (iv) Negative Logic
(v) Write D' Morgan's Theorems (vi) EPROM (vii) Totem Pole output

(b) Compare the Followings in every aspect. **07**

(i) TTL and CMOS (ii) RAM and ROM

Q:5 **(a)** Write short note on four bit Universal Shift Register. **07**

(b) Discuss the General State machine Architecture. **07**

OR

Q:5 **(a)** Explain the Fundamental Mode Model of Asynchronous State Machine with suitable example. **07**

(b) Write short note on Programmable Logic Arrays. **07**

****