

**GUJARAT TECHNOLOGICAL UNIVERSITY****MCA - SEMESTER-V • EXAMINATION – SUMMER 2017****Subject Code: 650012****Date: 08/06/2017****Subject Name: Software Development for Embedded System****Time: 02:30 PM-05:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a)** What is an embedded system? Explain the characteristics of embedded systems that distinguish such systems from other computing systems. **07**
- (b)** Define Following Terms:- **07**
1. Market Window
  2. CAN
  3. Timer
  4. Cross Compiler
  5. NRE Cost
  6. Design Metric
  7. Host Machine
- Q.2 (a)** List and define the three main IC technologies. What are the benefits of using each of the three different IC technologies? **07**
- (b)** List and define the three main processor technologies. What are the benefits of using each of the three different processor technologies? **07**
- OR**
- (b)** The d Using the revenue model compute the percentage revenue loss if  $D = 5$  and  $W = 10$ . If the company whose product entered the market on time earned total revenue of \$25 million, how much revenue did the company that entered the market 5 months late lose? **07**
- Q.3 (a)** Sketch the internal design of a  $4 \times 3$  ROM **07**
- (b)** Determine whether the following are synchronous or asynchronous: **07**  
(a) multiplexor, (b) register, (c) decoder.
- OR**
- Q.3 (a)** Four lights are connected to a decoder. Build a circuit that will blink the lights in the following order: 0, 2, 1, 3, 0, 2, .... Start from a state diagram, draw the state table, minimize the logic, and draw the final circuit. **07**
- (b)** Explain the assembler and cross assembler **07**
- Q.4 (a)** Explain short note and define- **03**
- Linker **03**
  - DMA **03**
  - FSMD **01**
- (b)** Explain internal structure of CCD in Digital Camera. **07**
- OR**
- Q.4 (a)** What is cache memory? Explain Direct Mapping and Fully Associative Mapping with diagram. **07**
- (b)** Briefly defines each of the following: mask-programmed EPROM, EEPROM, flash EPROM, SRAM, DRAM, PSRAM, and NVRAM. **07**
- Q.5 (a)** Describe tool chain for building embedded system. **07**
- (b)** Explain DBGMAIN.C, LEVELS.C and OVERFLOW.C. **07**
- OR**
- Q.5 (a)** What is Instruction Set Simulator? Explain all abilities of Instruction Set Simulators. **07**
- (b)** Explain Addressing modes in detail. **07**