Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-I Remedial Examination April 2010

Subject code: 710403 **Subject Name: ASIC Design**

Date: 08 / 04 / 2010 **Time: 12.00 noon -02.30 pm**

Total Marks: 60

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Write a VHDL program for full Subtractor using structural modeling. **06**

(b) Discuss VLSI design methodology in brief. **06**

Q.2 **(a)** Compare the following: **06**

I Moore and Melay machines.

II CPLD and FPGA

(b) Do as directed: **06**

I. Discuss the necessity of resolution function.

II. Compare VHDL language with C language.

III. Write predefined operators in increasing precedence.

OR

(b) Compare Inertial and Transport delay with suitable examples. **06**

Q.3 **(a)** Compare ROM, PAL, PLA, and PLD. **06**

(b) Implement following equation using structural and data flow modeling. **06**

Y= ABCD+ A'B'C' +B'C+ AD'

OR

Q.3 **(a)** Consider Melay Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "101" input bit sequence. Overlapping sequences are accepted, i.e." if input X is 1010100.....output Z is 0010100." Implement the state diagram for above and write VHDL code for it. **06**

(b) Discuss following terms: **06**

1. Moore's law 2. Gate density 3. Defect density

4. Yield 5. Gate Utilization 6. Die Cost.

Q.4 **(a)** Write VHDL code for the circuit that counts the number of positive clock edges contained within a signal "Indat". If count exceeds a " Threshold_Max" an overflow flag is set. **06**

(b) Discuss the following: **06**

1. Multiple processes and handshaking

2. Floor planning and placement

OR

Q.4 **(a)** State True/False. If statement is true justify it and if false correct it. **06**

1. Variable represents wire connection

2. Process statement itself is concurrent statement.

3. VHDL allows changing the loop index inside the loop.

4. A generic declares a constant object of mode IN.

5. It is not possible to mix three modeling styles in single architecture body.

6. "Case" statement is a sequential statement.

(b) Write VHDL codes using behavioural modeling for the following flip-flops with asynchronous clear input: **06**

I Negative edge-triggered D flip-flop

II J-K flip-flop

Q.5 **(a)** Write a VHDL code to generate clock with ON period of 15 ns and OFF period of 25 ns. **06**

(b) What are the main objectives of test bench? Discuss test bench with suitable examples. **06**

OR

Q.5 **(a)** Differentiate between "Exit" statement and "Next" statement. Explain the same by writing suitable VHDL code. **06**

(b) Discuss concurrent versus sequential signal assignment statement. What is the effect of Delta delay in VHDL? **06**

****