Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-I Examination January 2010

Subject code: 710403 Subject Name: ASIC Design

Date: 25 / 01 / 2010 Time: 12.00 – 2.30 pm

Total Marks: 60

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** List down the advantages and disadvantages of Finite State Machines. **06**

(b) Draw the basic block diagram of XC 9500 CPLD and Explain. **06**

Q.2 **(a)** Explain the ASIC Design flow in detail. **06**

(b) Explain the importance of Regularity, Modularity and Locality terms in ASIC Design. Take suitable example. **06**

OR

(b) Explain in brief (i) Full Custom ASICs (ii) Standard Cell Based ASICs (iii) Gate-Array Based ASICs. **06**

Q.3 **(a)** Write a VHDL code for 4-Bit Parallel-In-Serial-Out Shift Register. **06**

(b) Realize the following functions using PLA. **06**

$F_1 = \Sigma m (3,4,5,6,7,10,13,15)$

$F_2 = \Sigma m (2,4,6,8,10,14,15)$

$F_3 = \Sigma m (5,7,13,15)$

OR

Q.3 **(a)** Write a VHDL Code for 4 – Bit full – adder. Use structural modeling style. Take 1- Bit full adder as a component. **06**

(b) Define Mealy State Machine and Moore State Machine. Compare them. **06**

Q.4 **(a)** Explain Process statement. Explain the importance of sensitivity list. Quote suitable example. **06**

(b) Explain basic data types in VHDL. **06**

OR

Q.4 **(a)** Explain Assertion statement. Explain its usefulness in writing testbench. **06**

(b) What do you mean by Delta-delay ? Also explain Inertial Delay model and Transport Delay model. **06**

Q.5 **(a)** Write a short note on Anti-fuse and Static RAM programming technology. **06**

(b) Write a short note on operators used in VHDL. **06**

OR

Q.5 **(a)** Write a short note on Programmable Logic Devices (PLDs). **06**

(b) Explain Xilinx 3000 series logic cell, with configuration memory cell. **06**

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