Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. Sem. – IInd - Examination – June/July- 2011

Subject code:1722606

Subject Name: Algorithms for VLSI Physical Design Automation

Date:29/06/2011 **Time: 10:30 am – 01:00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain Full-custom layout in detail **07**

(b) Discuss unconstrained left-edge algorithm. **07**

Q.2 **(a)** Explain the following: **07**

(1) Sea of gates
(2) NP-Complete problem
(3) Deterministic and stochastic algorithms
(4) Floor planning
(5) Cross over in genetic algorithm
(6) Maze routers
(7) Horizontal constraint graph in channel routing

(b) Discuss Fiduccia-mattheyses heuristic algorithm for circuit partitioning. **07**

OR

(b) Discuss Lee algorithm in grid routing. **07**

Q.3 **(a)** The placement P shown in figure 1, three nets are given with different weight. N_1 = (*A,B,C*): W1=1, *N2* = (C,D, E): W2=3; ,N_3 = (D,F,G): W3=4. Compute X(P), Y(P) and L(P). **07**

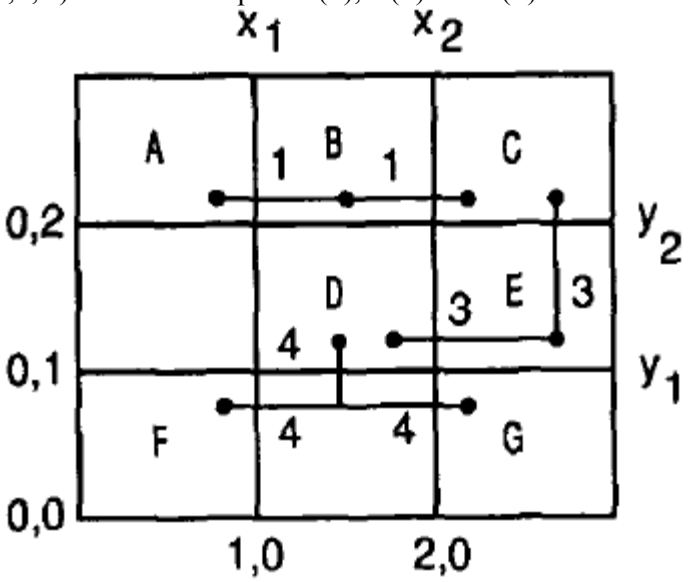

Figure 1

(b) What are the Optimization Objectives for placement? Describe various methods to estimate wirelength. **07**

OR

Q.3	**(a)**	In Layout generation list the different type of input source to a silicon compiler and explain any of them.	**07**
	(b)	Discuss the steiner tree problem in Global routing.	**07**
Q.4	**(a)**	Discuss Cluster growth algorithm for Floorplanning in brief.	**07**
	(b)	Discuss Graph representation of floorplans.	**07**
		OR	
Q.4	**(a)**	Explain criteria for channel crossing conversion and discuss conversion algorithm for Global routing.	**07**
	(b)	Discuss Hadlock's algorithm.	**07**
Q.5	**(a)**	Explain difficulties in physical design.	**07**
	(b)	Describe Kernighan-Lin algorithm in brief.	**07**
		OR	
Q.5	**(a)**	Discuss Genetic Algorithm for Placement.	**07**
	(b)	What is the need of Dogleg algorithm in channel routing? Describe Dogleg algorithm in detail.	**07**

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