

**GUJARAT TECHNOLOGICAL UNIVERSITY**M. E. I<sup>ST</sup> Semester–Remedial Examination – July- 2011**Subject code: 710422N****Subject Name : Digital Signal Processing and Applications****Date:15/07/2011****Time: 10:30 am – 01:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Define stable and causal system .Give an example of LTI system expressed by a difference equation. **07**
- (b) Differentiate between DTFT and DFT with the help of mathematical expressions. **07**
- Q.2** (a) Determine the Z-transform for the sequence  $x[n]=0.5^n u[n]$ .Specify its ROC also. **07**
- (b) Determine the inverse Z-transform using power series for  $X(z)=\ln(1-4z),|z|<1/4$ . **07**
- OR**
- (b) Determine the inverse Z-transform using long division for  $X(z)=(1-0.33z^{-1})/(1+0.33z^{-1})$  for a right sided sequence  $x[n]$ . **07**
- Q.3** (a) Describe properties of DFT. **07**
- (b) Explain circular convolution with the help of an example. **07**
- OR**
- Q.3** (a) Describe properties of DTFT. **07**
- (b) Explain linear convolution with the help of an example. **07**
- Q.4** (a) For the system function **07**
- $H(z)=(1+2z^{-1}+z^{-2}) / [1-(3/4)z^{-1}+1/3z^{-2}]$  ,draw flow graphs of all possible realizations for this system as cascade of first order systems.
- (b) Compute the DFT of the following finite length sequences considered to be of length N (N is even): **07**
- (i)  $x[n]=\delta[n]$
- (ii)  $x[n]=\delta[n-5]$
- OR**
- Q.4** (a) Give differences between DIT and DIF FFT algorithms. **07**
- (b) A continuous time signal is sampled at a sampling rate of 10 kHz and the DFT of 1024 samples computed. Determine the frequency spacing between spectral samples. Justify your answer. **07**
- Q.5** (a) Describe windowing method for FIR filter design. **07**
- (b) Compare FIR and IIR filter designs. **07**
- OR**
- Q.5** (a) Discuss DSP applications to radar engineering. **07**
- (b) With the help of a neat sketch, explain Digital Signal Processor architecture **07**

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