

GUJARAT TECHNOLOGICAL UNIVERSITYM. E. IST Semester–Remedial Examination – July- 2011**Subject code: 712602N****Subject Name: CMOS Circuit Design-I****Date:08/07/2011****Time: 10:30 am – 01:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Discuss Array Multiplier in detail. **07**
 (b) Describe MOS Small signal Model **07**
- Q.2** (a) Explain the following: **07**
 (1) Channel Length Modulation
 (2) Performance parameters of an Op-amp
 (b) Discuss Dynamic Power consumption of CMOS inverter **07**
- OR**
- (b) Describe CASCODE current mirrors in detail. **07**
- Q.3** (a) Discuss Carry bypass adder in detail. **07**
 (b) Discuss Power reduction method in Standby (or sleep) mode. **07**
- OR**
- Q.3** (a) Discuss Multipole Systems for stability and frequency compensation. **07**
 (b) Explain large signal analysis of active current Mirror. **07**
- Q.4** (a) Derive small signal voltage gain for common-source stage with resistive load. **07**
 (b) Discuss Qualitative analysis of differential pair. **07**
- OR**
- Q.4** (a) Discuss frequency response of source follower amplifier. **07**
 (b) Discuss Dual of Miller's theorem. **07**
- Q.5** (a) Derive the voltage gain of common gate stage. **07**
 (b) Discuss Gilbert cell. **07**
- OR**
- Q.5** (a) Discuss Two stage Op-amps. **07**
 (b) Calculate the input common mode voltage range and the closed-loop output impedance of the unity gain buffer. Assume threshold voltage of each device is 0.7 volt and an overdrive voltage of 0.3 volt. **07**
